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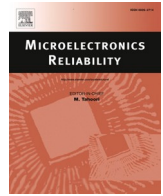
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Research Paper

Design-of-Experiments and ALT plan for reliability qualification of chip resistors based on mission profile of AIMDs[☆]

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A B S T R A C T

Chip resistors are integral components of electronic devices, including Active Implantable Medical Devices. This work, as part of RECOME project, is focusing on developing a methodology for defining accelerated life test plans to qualify chip resistors as per the mission profile of AIMDs. This will be done by combining design of experiments and accelerated life tests associated with failure mechanisms. Defining test protocols, such as thermal cycling, will be a critical component of this work.

1. Introduction

Active Implantable Medical Devices (AIMDs), including pacemakers and cochlear implants, have become an essential part of many patients' lives. The integration of electronics into these devices enables improved monitoring and seamless integration. However, there is a lack of standards that keep up with this technological advancement. Generally, AIMDs are qualified based on experiences in other sectors, such as aviation [1] and military. The absence of a "medical grade" specific to electronic components for AIMDs calls for mastering the reliability of these components with respect to AIMDs' mission profile [2], especially the commonly used ones such as resistors.

This work is carried out in the framework of the RECOME project (Reliability of Electronic Components for MEDical applications) which aims to provide a guide for reliability qualification of electronic components used in AIMDs, with a special attention given to miniature components (0201 and 01005 in metric size code). Particularly, this study proposes a methodology to define qualification tests of chip resistors based on a Design-of-Experiment (DoE). First, Section 2 explains briefly the FMMEA (Failure Modes, Mechanisms, and Effects Analysis) and how test protocols are defined. Section 3 goes over the failure analysis of some of the resulting failed chip resistors. Section 4 explains the results analysis and discusses the different issues related to reliability testing. Finally, Section 5 concludes with a reminder of the general perspectives.

2. Device and stress procedure description

Reliability of chip resistors can depend on various design factors related to the manufacturing of the component. To establish the relationship between these factors and the desired output, DoE methods can be applied (e.g., Taguchi designs) [3]. Firstly, field experience of TRONICO enriched with a study of the state-of-the-art facilitated the identification of the most critical design factors impacting reliability and quality [4] [5]: technology (thick film or thin film), size of the component, and resistance value.

Table 1 illustrates an example of the defined designs of experiments. As shown in Fig. 1, 24 components shall be tested for every combination of design factors (every line of the experimental design). The chosen components hold the "automotive grade" label and have already qualified under the AEC-Q200 standard [6]. Thus, the FMMEA is oriented toward observing the defects of these components, rather than the ageing, given their high reliability. The failure mechanisms are categorized according to the environmental factors that accelerate failure to define test plans.

To generate the qualification test plan for chip resistors, the procedure is as follows:

1. Elaborate the mission profile of AIMDs.
2. Identify the critical failure mechanisms of concern for chip resistors with respect to the mission profile of AIMDs.
3. Calculate the acceleration factors related to critical environmental stresses, based on literature.

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Table 1

Results of accelerated life tests for each combination of technological factors of miniature chip resistors (Factors are: A) Film material, B) Size, C) Resistance value, D) Manufacturer; ALTs are: TC - Thermal Cycling, EO - Electrical Overload).

DoE combination	A	B	C	D	Number of failures (/24)		
					T	T	E
					C	C	O
Run N°01	Thick	0201	10Ω	1	0	0	0
Run N°02	Thick	0201	10KΩ	1	0	0	0
Run N°03	Thick	0201	100KΩ	1	0	0	5
Run N°04	Thick	0201	10Ω	2	0	0	0
Run N°05	Thick	0201	10KΩ	2	0	0	0
Run N°06	Thick	0201	100KΩ	2	0	0	0
Run N°07	Thick	0201	10Ω	3	0	0	0
Run N°08	Thick	0201	10KΩ	3	0	1	0
Run N°09	Thick	0201	100KΩ	3	0	0	0
Run N°10	Thick	01005	10Ω	1	3	0	0
Run N°11	Thick	01005	10KΩ	1	1	0	1
Run N°12	Thick	01005	100KΩ	1	0	0	4
Run N°13	Thick	01005	100Ω	2	0	0	0
Run N°14	Thick	01005	10KΩ	2	0	0	0
Run N°15	Thick	01005	100KΩ	2	0	0	0
Run N°16	Thick	01005	10Ω	3	0	0	0
Run N°17	Thick	01005	10KΩ	3	1	0	1
Run N°18	Thick	01005	100KΩ	3	0	0	0

N.B.: The number of each run is only for reference with respect to the combinations of the designs of experiments. The designed experiments themselves are conducted in random order, an important aspect of Taguchi designs.

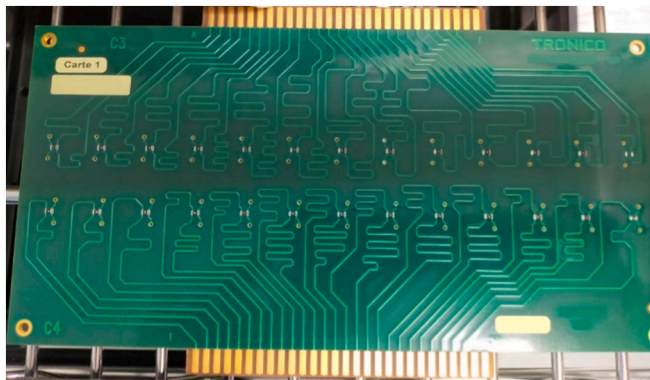


Fig. 1. An example of PCB with 24 similar chip resistors mounted.

4. Quantify the test metrics (e.g., stress time, sample size) based on mission profile and calculated acceleration factors.

Due to the high reliability and technological maturity of resistors, the goal of the accelerated tests in this study will be to detect latent quality defects. Therefore, the FMMEA will be oriented toward identifying failure mechanisms related to quality defects.

Chip film resistors can fail due to different types of environmental loads such as: mechanical stress [7], overcurrent/overvoltage stress [7], humidity [8] [9], power cycling [10]. This is through several mechanisms, including:

- Corrosion: The deterioration of the protective coating allows moisture to penetrate, causing electrolytic corrosion of the resistive element (e.g., NiCr in thin-film resistors). This may lead to increased resistance or an open circuit.
- Fatigue Fracture: Localized defects in the resistor’s etched pattern, such as notches, bridge defects, or embedded non-conductive particles, can cause hot spots. Power cycling induces thermo-mechanical fatigue, leading to cracks that increase resistance or cause an open circuit.
- Electrode Separation: This occurs when the intermediate electrode separates from the internal electrode due to mechanical stresses such as excess solder, excessive thermal impact, or resin compression. This results in increased resistance or an open circuit.
- Solder Cracking: Thermal stress due to differences in the coefficient of thermal expansion between the PCB and the resistor can cause solder fatigue, leading to cracks that increase resistance or cause an open circuit.
- Resistive Element Damage: Electrical overloads, excessive electrostatic discharge (ESD), or surge pulses can generate heat, particularly at localized defects, damaging the resistive element and leading to increased resistance or an open circuit.

Based on the FMMEA it is evident that multiple types of ALTs are necessary to detect common failure mechanisms in chip film resistors. The AEC-Q200 standard [6] covers many classical life tests related to common failure modes, but combining some of these tests can improve the chances of observing failures. For example, thermal cycling combined with humidity under bias can increase stress on components to detect a protective coating defect leading to corrosion due to penetration of humidity into the resistor. Additionally, overvoltage stress-inducing tests like Electrical Overload, which are not considered in AEC-Q200, are essential to capture specific failure modes.

From the FMMEA analysis, two types of tests were selected to address the common resistor failures:

1. Thermal cycling, including humidity, to target thermo-mechanical stress and corrosion (Fig. 2).
2. Electrical overload to induce failures related to fatigue fractures and resistive element damage (Fig. 3).

Thermal cycling combined with humidity is particularly designed to highlight quality defects by inducing failures from mechanical stresses and corrosion. The FMMEA also notes that miniaturization increases the risk of corrosion, leading to the definition of two profiles for small resistors (01005 and 0201), with varying high temperatures and humidity levels to study corrosion. Larger resistors (0402 to 1206) will follow a unified profile.

On the other hand, electrical overload tests, as shown in Fig. 3, are implemented to observe failures related to fatigue and resistive element damage.

Resistance drift is used as the electrical parameter to monitor the degradation of resistors, and acceptable drift values are specified in the manufacturer’s datasheets for each component, which are originally taken from standards.

Fig. 2 shows the thermal cycling profile for miniature chip resistors. This profile is based on the standard MIL-STD-883 Method 1031 [11] since it is intended for thin film conductors and resistors in highly corrosive environment (human body). Electrical parameters (resistance) are to be measured during the 12 h following the test according to the same standard. The chip resistors during each thermal cycle will enter a period of biasing which coincides with the application of humidity. This is to provide enough bias to accelerate electrochemical migration or corrosion without the bias being the stress factor directly provoking the failure mechanisms. Therefore, the chip resistors are biased in voltages and currents lower than their ratings.

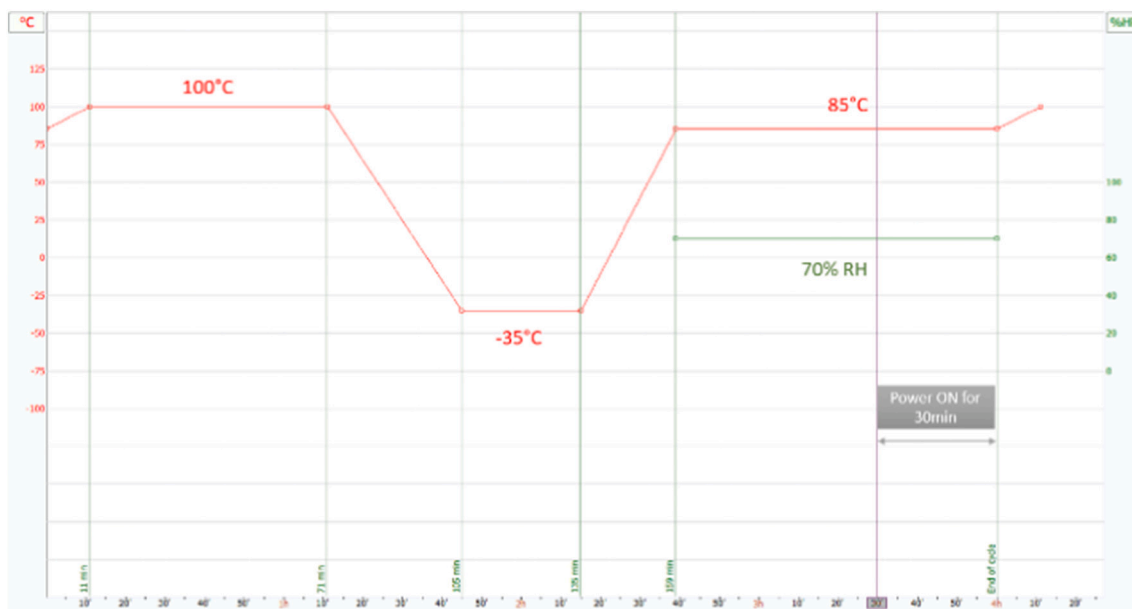


Fig. 2. Thermal cycling profile for 0201 and 01005 film resistors.

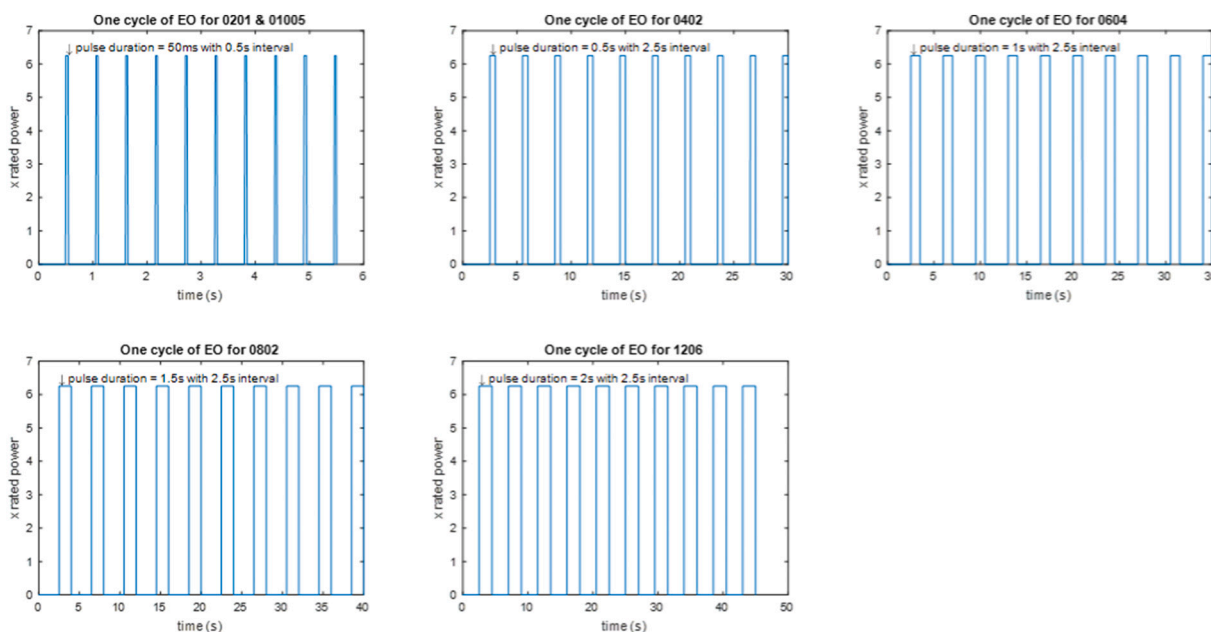


Fig. 3. Electrical overload cycles.

3. Failure analysis

Results of the tests conducted on miniature chip resistors are reported in Table 1. Failures are recorded when the resistance value difference between before and after the test drifts beyond the specified tolerance in the standards.

An analysis of failure was conducted for each of the failed resistors. This analysis started with a visual examination using an optical microscope and was followed by the use of other failure analysis tools when necessary. To illustrate, an examination, through optical microscopy, of the resistors corresponding to run N°03 (crossed with EO test), which exhibits the highest number of failures (see Table 1), reveals the presence of holes indicated by a red circle in Fig. 4, which were observed to have developed on the protective coating.

It is possible that the damage to the resistive element was caused by

localized fusing during the electrical overload. Additionally, some gray area exists in the borders of the protective coating near the terminations. To investigate both observations, an X-ray analysis was conducted, the results of which are presented in Fig. 5.

An examination of the X-ray image of the same component reveals the presence of several small white spots. It is assumed that these are voids resulting from the trapping of air within the solder joints during the manufacturing process. Such voids may be implicated in localized heating and uneven heat dissipation. To further investigate the aforementioned hole, the component was subjected to micro-sectioning in steps in parallel with optical microscopy at each step (see Fig. 6 for an example). However, no peculiarities were observed. It can be concluded for this particular component that the observed resistance value drift was potentially caused by damage to the resistive element resulting from localized heating.

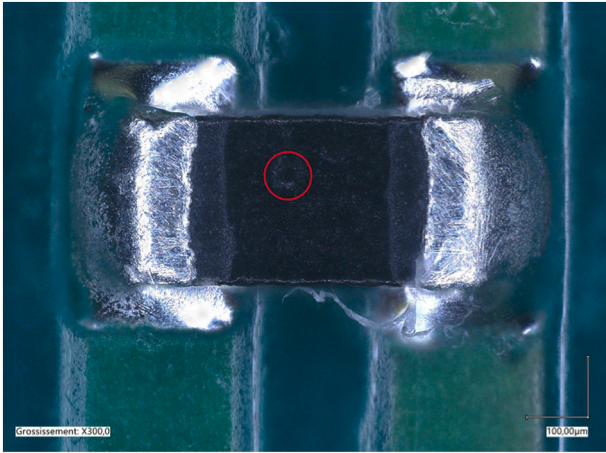


Fig. 4. Optical microscope image of a failed chip resistor (run N°03).

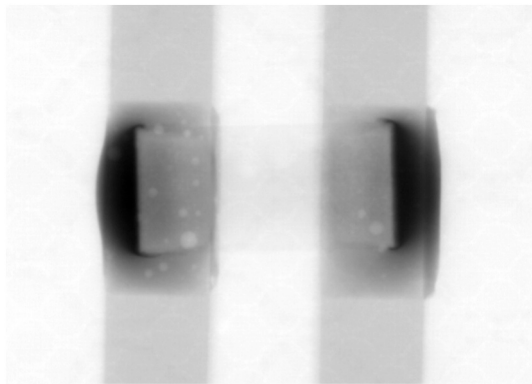


Fig. 5. X-rays image of a failed chip resistor (run N°03).

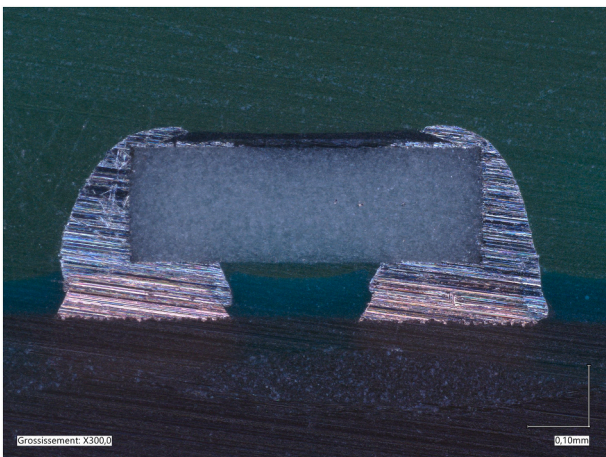


Fig. 6. Microsection image of a failed chip resistor (run N°03).

Likewise, some failed components that showed discoloration under optical microscopy were analyzed using scanning electron microscopy and energy-dispersive X-ray spectroscopy (SEM-EDS) to identify any anomalies related to corrosion resulting from the thermal cycling profiles. However, no abnormalities were observed in the material composition of the component. Therefore, it can be assumed that the dominant failure mechanism in this work for the electrical overload test is localized heating around quality defects and the dominant failure mode is resistance value drift.

4. Data and results discussion

Different tools can be employed to statistically analyze the relevance of these results, focusing on two primary questions:

1. What combinations of controllable factors are most robust against the ALTs?
2. Which type of ALT is most effective at discerning potential failures?

To answer these questions, the following analyses will be done on the Taguchi DoE from Table 1:

- Calculation of the signal-to-noise ratio for each row (of the inner array), then for each column (of the outer array). This is to identify the effects of the factors on location and dispersion (confounding both effects), as well as the effects of ALTs.
- Calculation of the mean of each combination, followed by the effect of each factor on the mean. The theoretical mean is then calculated for each combination to identify location effects.
- Repetition of the previous step for the variance instead of the mean to identify dispersion effects.

In this example, the response of interest is the number of defects, and the desired response depends on the objective as will be explained in the following sub-sections.

4.1. Response of cross array design

Due to the high reliability of chip resistors, it is quite natural for the tests to produce a very small number of failures, or even none. In this case, and to avoid calculation problems in the application of the statistical methods that will be discussed below, the limits of the upper one-sided confidence interval p_{sup} of the proportion of defected components in a sample can be used as the response of the crossed array design rather than the number of defects. It is calculated by solving the following equation [13]:

$$\sum_{k=0}^{N_d} \binom{N}{k} p_{sup}^k (1 - p_{sup})^{N-k} = \alpha \tag{1}$$

where N is the sample size, N_d is the number of defected components in a sample, and α is the risk level.

4.2. Analysis of the inner array

The objective of the inner array analysis is to understand the impact of technological factors on component failure, particularly the sensitivity of the component to noise factors (and thus its robustness to environmental conditions). To achieve this, the mean and variance of responses for each combination in the inner array can be analyzed by calculating the corresponding theoretical values, as explained by the theoretical model below.

Let k be a factor in the Taguchi design, n_k the number of levels of this factor, and i the index of the combination of the inner array DOE_i . F_{ki} is a unit vector of dimension $1 \times n_k$ that contains the levels of factor k such that only the element corresponding to the level of the factor present in the DOE_i combination equals 1, while the rest of the elements are 0. E_k is a vector of dimension $n_k \times 1$ containing the effects of each level of factor k . \bar{Y} is the average of all responses. The associated theoretical model is:

$$\tilde{Y}_i = \bar{Y} + \sum_{k=1}^p E_k F_{ki}$$

The theoretical response \tilde{Y}_i is calculated using the mean and variance, and the results are analyzed in relation to the inner array combinations.

The previous method allows us to obtain the position effects, which

refer to the influence of controllable factors on the central position of the response distribution (measured by the theoretical mean), as well as dispersion effects, which concern the variation of the response (measured by the theoretical variance).

The variances are calculated over the mean of the response for every combination of the ALT since the interest lies in the variability over the controllable variables.

To combine position and dispersion effects into a single indicator, Taguchi proposes calculating the signal-to-noise ratio [12].

Let Y_{ij} be the response associated with the combination (DOE_i, ALT_j) . The objective is to identify the combination DOE_i , which is associated with the smallest number of failures, thereby minimizing the loss in response caused by noise factors. To do this, Taguchi suggests calculating the function [14]:

$$S / N_i = -10 \log \left[\frac{1}{n_i} \sum_{k=1}^{n_i} Y_{ij}^2 \right] \tag{2}$$

It is important to note that here, the signal refers to the desirable response (which related to the number of observed defects in the components), while the noise refers to the undesirable variability induced by the uncontrollable factors (environmental stresses through the accelerated life tests). Thus, the signal-to-noise ratio (S/N) represents the robustness of a response to noise, and the desired result is always a high S/N , whether the desired response is a maximum, a minimum, or a certain value. Consequently, whatever the objective, the value to seek during the analysis is the maximum S/N .

4.3. Analysis of the outer array

The objective of the outer array analysis is to understand and distinguish the effect of environmental factors on the failure of the component, particularly to find the combination ALT_j that is most effective for detecting defects while being the least sensitive to variations in technological factors. Consequently, the objective is to identify the maximum response. In this case, the function used is [14]:

$$S / N_j = -10 \log \left[\frac{1}{n_c} \sum_{k=1}^{n_c} \frac{1}{Y_{ij}^2} \right] \tag{3}$$

By examining the theoretical values of the mean and standard deviation displayed in columns C12 and C13 of Table 2, it is observed that the miniature resistors manufactured by manufacturer 1, with a resistance value as high as that of 100kΩ, are associated with a relatively high proportion of defects and an increase in variance. In contrast, the resistors manufactured by manufacturer 2, with resistance values as low as 10 Ω, are the most robust to ALTs.

Example of calculating the theoretical mean for combination DOE No. 06:

Table 2

Results of statistical calculations on the reduced Taguchi design (one-sided confidence bound of the true failed proportion at the 95 % confidence level).

Combination DOE (i)	A	B	C	D	Upper one-sided confidence bound (p_{sup})			S/N	\overline{p}_{sup}	Var(p_{sup})	$\overline{\overline{p}}_{sup}$	$\sqrt{\overline{\overline{Var}}(p_{sup})}$
					TC1	TC2	EO2					
Column 1	Column 2	Column 3	Column 4	Column 5	Column 6	Column 7	Column 8	Column 9	Column 10	Column 11	Column 12	Column 13
N°01	Thick	0201	10Ω	1	0.14	0.14	0.14	25.96	0.14	0.000	0.17	0.07
N°02	Thick	0201	10KΩ	1	0.14	0.14	0.14	25.96	0.14	0.000	0.18	0.07
N°03	Thick	0201	100KΩ	1	0.14	0.14	0.42	20.41	0.24	0.017	0.19	0.09
N°04	Thick	0201	10Ω	2	0.14	0.14	0.14	25.96	0.14	0.000	0.13	0.03
N°05	Thick	0201	10KΩ	2	0.14	0.14	0.14	25.96	0.14	0.000	0.14	0.04
N°06	Thick	0201	100KΩ	2	0.14	0.14	0.14	25.96	0.14	0.000	0.15	0.05
N°07	Thick	0201	10Ω	3	0.14	0.14	0.14	25.96	0.14	0.000	0.14	0.03
N°08	Thick	0201	10KΩ	3	0.14	0.21	0.14	24.50	0.17	0.001	0.15	0.04
N°09	Thick	0201	100KΩ	3	0.14	0.14	0.14	25.96	0.14	0.000	0.16	0.05
N°10	Thick	01005	10Ω	1	0.32	0.14	0.14	22.18	0.20	0.007	0.19	0.07
N°11	Thick	01005	10KΩ	1	0.21	0.14	0.21	23.41	0.19	0.001	0.19	0.07
N°12	Thick	01005	100KΩ	1	0.14	0.14	0.37	21.24	0.22	0.012	0.20	0.10
N°13	Thick	01005	100Ω	2	0.14	0.14	0.14	25.96	0.14	0.000	0.14	0.03
N°14	Thick	01005	10KΩ	2	0.14	0.14	0.14	25.96	0.14	0.000	0.15	0.04
N°15	Thick	01005	100KΩ	2	0.14	0.14	0.14	25.96	0.14	0.000	0.16	0.05
N°16	Thick	01005	10Ω	3	0.14	0.14	0.14	25.96	0.14	0.000	0.15	0.02
N°17	Thick	01005	10KΩ	3	0.21	0.14	0.21	23.41	0.19	0.001	0.16	0.03
N°18	Thick	01005	100KΩ	3	0.14	0.14	0.14	25.96	0.14	0.000	0.17	0.06
Row 21				S N	-15.19	-15.54	-14.93	Mean	0.16	0.002		

TC1: is the first thermal cycling, TC2: is the second thermal cycling, EO: is the electrical overload test.
S/N: signal-to-noise ratio.

\overline{p}_{sup} , Var(p_{sup}): are the mean and the variance of the upper one-sided confidence bound (p_{sup}).

$\sqrt{\overline{\overline{Var}}(p_{sup})}$: is the theoretical standard variation of p_{sup} .

$\overline{\overline{p}}_{sup}$: is the theoretical mean of p_{sup} .

$$\begin{aligned} \tilde{Y}_{06} = \bar{Y} + E_{A1} + [E_{B1} \ E_{B2}] \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \\ [E_{C1} \ E_{C2} \ E_{C3}] \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} + [E_{D1} \ E_{D2} \ E_{D3}] \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \end{aligned} \quad (4)$$

This yields after replacing with numerical values:

$$\begin{aligned} \tilde{Y}_{06} = 0.16 + 0 + [-0.00630 \ 0.00630] \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \\ \tilde{Y}_{06} = 0.16 + 0 + [-0.00630 \ 0.00630] \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \\ [-0.00911 \ -0.00008 \ 0.00919] \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} + \\ [0.02688 \ -0.01917 \ -0.00771] \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} \\ = 0.15 \end{aligned} \quad (5)$$

The effects are calculated for each level of each factor. For example, the effect of level 2 of factor D (which corresponds to the effect of manufacturer 2 is:

$$E_{D2} = \frac{Y_{04} + Y_{05} + Y_{06} + Y_{13} + Y_{14} + Y_{15}}{6} - \bar{Y} \quad (6)$$

4.4. Results discussion

On the other hand, signal-to-noise ratios (S/N) are calculated for each row across the three types of ALTs. In this case, the interest is in the minimum value of the response (to answer question 1). Similarly, for each type of ALT across the combinations, the interest is in the maximum value of the response (to answer to question 2). In either case, the goal is to maximize S/N (highlighted in green). The results mainly show that Electrical Overload enables better detection of defects in chip resistors.

For highly reliability electronic components like chip resistors, intrinsic failure during accelerated life tests is expected to be related to latent defects (defects that are not easily noticeable, and which escaped screening tests). The detection of these, as opposed to observing degradation, will require relatively higher levels of environmental stresses and shorter durations with less frequent measurements of electrical parameters. Indeed, defects are more susceptible to be observed, if at all, during earlier cycles while ageing is more prone to occur later after long enough accumulative cycles. Therefore, it was crucial to deeply understand the failure mechanisms of chip resistors and the relevant defects that are susceptible to happen in the context of AIMDs. Using automotive qualified components AEC-Q200 [6] ensures a guaranteed level of reliability and focusing solely on failure mechanisms associated with the distinct AIMD environments.

5. Conclusions

This study covers various points which can be summarized as follows:

- The design of accelerated life tests for chip resistors based on the mission profile of AIMDs and the failure mechanisms of chip resistors.
- With standards and predictive reliability guides as a starting point, test protocols were developed to target the defects of chip resistors

relevant to mission profile, such as thermal cycling combined with humidity and on/off power cycling.

- The effects of technological factors of the components (e.g., size, resistance value) were accounted for through Taguchi design of experiment, with an emphasis on miniaturization.

The ultimate objective is to offer a methodology to select accelerated tests for qualifying chip resistors. A methodology that is rooted in understanding the failure mechanisms of these components, especially in relation to the mission profile of AIMDs, and which takes into consideration the effects of technological factors through the use methods of design of experiments.

Finally, thanks to Taguchi design of experiments approach, this work has enabled a selection of Electrical Overload as an additional accelerated life test to implement in addition to typical accelerated life tests to qualify miniature chip resistors for AIMDs.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Fatima-Ezahra INDMESKINE reports financial support was provided by University of Angers. Fatima-Ezahra Indmeskine reports financial support was provided by French Ministry of Economy Finance and Recovery. Fatima-Ezahra Indmeskine reports financial support was provided by Pays de la Loire Academic Region. Fatima-Ezahra Indmeskine reports a relationship with University of Angers that includes: employment. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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