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Jaber Al Rashid, Mohsen Koohestani, Laurent Saintis, Mihaela Barreau. Lifetime reliability modeling on EMC performance of digital ICs influenced by the environmental and aging constraints: A case study. *Microelectronics Reliability*, 2024, *Microelectronics Reliability* 159 (2024), 159, pp.115447. <10.1016/j.microrel.2024.115447>. <hal-04622696>

HAL Id: hal-04622696

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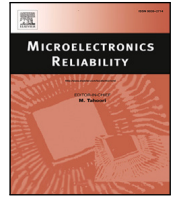
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Research paper

Lifetime reliability modeling on EMC performance of digital ICs influenced by the environmental and aging constraints: A case study

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ARTICLE INFO

Keywords:

Lifetime reliability
Accelerated degradation tests
Generalized Eyring model
EMC conducted immunity testing
Maximum likelihood estimation

ABSTRACT

This paper aims to develop the lifetime reliability model on electromagnetic compatibility (EMC) performance of the Atmel Attiny85 microcontroller integrated circuit (IC) chip samples, depending on the observed variation of the conducted immunity to the electromagnetic interference imposed by the combined influence of various environmental and aging (i.e., thermal and electrical voltage stress) constraints. A constant-stress accelerated degradation tests plan was designed and implemented by applying different constant thermal (i.e., 70 and 110 °C) and electrical voltage (i.e., 4 and 5 V) stress magnitude levels simultaneously in various multiple stress combinations. Direct power injection (DPI) conducted immunity tests were performed in nominal condition on all the programmed device under test (DUT) samples in both the fresh and aged states at various stress time duration. The best-fit EMC degradation paths were generated using regression analysis, followed by evaluating the pseudo time-to-failure (*TTF*) data and estimating the unknown parameters of the developed degradation path model. The performance metrics for lifetime reliability were evaluated by combining the Weibull distribution function with the generalized Eyring accelerated life test model. The maximum likelihood estimation method was utilized to estimate the relevant reliability model parameters. The developed reliability model was found to have the capability to estimate the electromagnetic unreliability against the lifetime *TTF* data of all the selected DUT samples with good precision and acceptable accuracy in both nominal and aging stress conditions. It is demonstrated that the non-failure probability of the DUT samples would remain at 1 for the first 1200 h, and that, under nominal conditions, the prediction of corresponding *TTF* data for all of those IC samples would fluctuate between 1400 and 1600 h.

1. Introduction

The EMC performance of both analog and digital ICs can have significant impact on the lifetime reliability due to exposure to the harsh environmental conditions. Such ICs comprise embedded circuits, including microcontroller ICs, and their operations are impacted by the injection of continuous-wave and transient electromagnetic (EM) disturbance signals. In [1], the conducted immunity behavior of the analog to digital converter circuits was assessed based on the proposed failure criteria to identify both linear and non-linear distortion caused by the electromagnetic interference (EMI). The DPI test was performed in [2] to assess the EMC performance of digital ICs up to 1 GHz, specifically dedicated to various non-volatile SPI EEPROM memory devices. A systematic immunity analysis based on resonance was conducted in [3] on different types of microcontrollers to identify conducted immunity determinant factors, contributing to the universal model construction to

predict the conducted immunity of those tested ICs. In [4], conducted immunity modeling approach of the digital core within the IC chip was presented and validated by comparing the simulated results of the developed model to that of the measurements performed by conducting the DPI test.

The transient EM conducted immunity was also characterized by performing the electric fast transient (EFT) test on various analog and digital circuit blocks embedded within the IC chip. In [5,6], the EFT tests was performed on the tested microcontroller ICs to investigate the conducted susceptibility level of various analog and digital input/output (I/O) and power supply pins of to the EFT pulse in the time-domain and identify different failure modes involved for causing the observed IC failure and/or malfunction. Different methodological approaches were applied to develop and simulate both the conducted

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<https://doi.org/10.1016/j.microrel.2024.115447>

Received 30 April 2024; Received in revised form 3 June 2024; Accepted 15 June 2024

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immunity and emission models, which were compared to the conducted immunity measurements of the custom designed digital IC chips under the influence of aging stress conditions [7]. An electrical overstress stress aging condition was applied in [8,9] to evaluate the conducted emission (CE) level measurements of both fresh and aged digital circuits, designed in a CMOS 90 nm technology chip.

An IC is expected to operate consistently in an EM environment, without any failures for an extended period of its lifetime. Degradation of an IC's EMC within an electronic component or system may occur due to the influence of external environmental conditions, resulting in a significant decline in the functional performance of that component over time, and consequently its lifespan and reliability based on the user-defined soft failure threshold criterion [10]. Various aspects of degradation modeling and reliability prediction methods were discussed in [11], demonstrating the time-dependent degradation process could be modeled mathematically to predict the failure time data, probability of failure and reliability of the degraded component within a system. In [12], similarities, differences, advantages and disadvantages of different types of degradation modeling approaches, such as the model-based and data-driven (i.e. physics-based, gamma, and wiener processes) for the reliability assessment were discussed. In [13], existing literature studies on employing degradation modeling approaches for digital logic circuits were reviewed, proposing analytical mathematical models and the application of CAD software simulation tools to estimate the aging impact on the functional performance degradation of FPGAs, ASICs, processors and SRAM based memory devices.

Accelerated life tests (ALTs) were performed on electronic component and system by applying accelerated stress factors (i.e., temperature and electrical overstress) to obtain the test data, which could be utilized to predict the relevant reliability metrics in nominal condition by employing various developed appropriate stochastic and/or empirical models to extrapolate those measured data [14]. Based on the measured functional performance characteristic degradation data, various kinds of reliability estimation modeling techniques were proposed followed by performing analysis to predict lifetime and unknown reliability parameters of those developed models for a complex system [15], thin film capacitors [16], rectifier [17], RF relays [18], bidirectional high voltage DC to DC converter [19] and FPGA embedded chip [20], analog CMOS voltage regulator circuit [21]. In [22], physics-based modeling approach was considered to develop the EMC lifetime reliability model was developed to estimate the necessary model parameters and predicted failure time of the tested analog ICs based on the step-stress thermal stress accelerated degradation test (ADT) plan, based on the EMC performance evolution under the accelerated step-stress aging conditions.

Previous research studies compared the EMC performance degradation of digital ICs before and after aging tests to evaluate the impact of applying either thermal and/or electrical voltage stress conditions. However, the evolution of conducted immunity to EMI at various stress time intervals to generate EMC degradation paths, as well as the application of statistical methods for developing reliability models based on measured degradation data to predict the necessary EM lifetime reliability metrics have not yet been investigated. With the aim to study and develop degradation and lifetime reliability models for ICs subjected to the combined influence of constant thermal and electrical voltage aging stress conditions in various combinations specified by the ADT plan, since, to the best of our knowledge, such models have been so far developed for analog and digital circuits based on the long-term evolution of conducted emission. Thus, those models are developed in the current study based on the conducted immunity performance degradation of the studied ICs using suitable acceleration law combined with the Weibull distribution, which would allow for the prediction of reliability parameters in both nominal as well as tested and/or untested stress conditions.

This paper is divided into following sections. Section 2 highlights the designed ADT plan for the tested IC samples. Section 3 provides a

Table 1

Accelerated aging constant stress ADTs plan of the Attiny85 ICs for total stress duration of 1000 h.

| IC samples | Thermal stress (°C) | Electrical voltage stress (V) |
|------------|---------------------|-------------------------------|
| AT1-AT6 | 110 °C | 4 V |
| AT7-AT12 | 110 °C | 5 V |
| AT13-AT18 | 70 °C | 4 V |
| AT19-AT24 | 70 °C | 5 V |

detail procedures on the experimental test setup followed by demonstrating the conducted immunity measurement results in Section 4. Finally, the degradation path and reliability modeling approach and its analysis are presented in Sections 5 and 6, respectively.

2. Constant stress ADT plan

The constant stress ADT plan was designed to trigger the relevant failure modes and mechanisms by accelerating the aging of the digital circuit embedded within the Attiny85 microcontroller ICs based on the selection of multiple stress factors (i.e., temperature and electrical voltage), stress magnitude, and total duration. The number of IC samples selected for ADT under the influence of both temperature and electrical voltage stress is detailed in Table 1. A total of 24 IC samples (i.e., AT1-AT24) were considered to obtain an accurate enough estimation of the observed conducted immunity performance degradation caused by simultaneously applying two different constant temperature (i.e., 110 °C and 70 °C) and electrical voltage stress levels (i.e., 4 V and 5 V).

Among the tested IC samples, the selected 12 DUT samples (i.e., AT1-AT12) were subjected to the highest constant temperature stress with two distinct constant electrical voltage stress magnitudes for a total stress duration of 1000 h. For the remaining IC samples (i.e., AT13-AT24), a similar constant stress ADT was developed, taking into account two different electrical voltage aging stress levels applied for the same total stress period, but employing a lower constant temperature stress level (i.e., 70 °C) compared to those IC samples (i.e., AT1-AT12) under test. It should also be noted that some additional samples were also examined in their fresh state. The DPI test results obtained from those samples were found to be consistent and comparable to those obtained from the tested DUT samples (AT1-AT24), which might be regarded as the reference samples. It is also worth mentioning that the DPI test setup condition was remained entirely unchanged throughout the entirety of the measurement campaign. It is noteworthy that all IC samples experienced failure after 200 h of aging when subjected to high thermal stress level of 110 °C and input biasing voltages exceeding 5 V. As a result, to ensure that the aged samples would not undergo into permanent failure throughout the total stress duration of the ADTs, the electrical voltage stress levels were estimated to be 33.3% and 66.7% greater than the nominal biasing voltage of 3 V, which was accounted for in the ADT plan.

3. Materials and methods

This section presents the developed algorithm for testing the Attiny85 IC sample as well as the accelerated aging experimental methodology to implement the designed constant stress ADT plan for characterizing the conducted immunity performance of both fresh and aged IC samples, subjected to multiple stress factors of varying stress magnitudes at various stress duration. It also provides the detail experimental procedures implemented to characterize the conducted immunity performance evaluation for both fresh and aged Attiny85 IC samples at various stress time duration.

3.1. Attiny85 IC under test

Attiny85 is a low power and high performance 8-bit microcontroller IC chip, which is composed of both analog and digital circuit blocks, including various functional specifications as mentioned in [23]. Using the Arduino UNO as the in-system programmer (ISP), the developed program was uploaded onto the IC's flash programmable memory. This IC chip was programmed by implementing the required algorithm necessary to exhibit the desirable functionality of the digital logic circuit under nominal conditions (i.e., 25 °C and 3 V). The latter was accomplished by following the step-by-step procedures to execute this algorithm for obtaining the expected functioning of this digital IC sample.

1. Initialize various input and output ports of the Attiny85 microcontroller. The digital input (DI) and serial clock (SCK) pins are configured as inputs to receive both the DI and SCK square-wave signals from an external functional signal generator, while the digital output (DO) pin is set as an output to generate the DO square-waveform signal. The initial state of both the DI and DO pin were set at the digital logic low (bit 0) voltage level.
2. The program's void loop() method allows to wait until the digital square-wave signal associated to the SCK pin changes from logic low (bit 0) to logic high (bit 1) level (rising edge), assuring clock signal synchronization.
3. Read the initial logic state (bit 0) of the digital input signal on the DI pin and store the digital value (logic low) in the data variable, which then sends the data to the DO pin so that its state matches that of the DI pin state (i.e., if the DI bit is 1, the DO bit also sets to high).
4. Using the 'while()' loop function in the code, check and wait for detecting for the rising edge of the external clock signal on the SCK pin.
5. Record the previous state value of the DO pin at the rising edge of the clock pulse.
6. Wait for detecting the next falling edge of the clock signal applied to the SCK pin, followed by the next rising edge.
7. At the ascending edge of the clock signal, determine whether the DO pin was previously at a logic low or high voltage level. If the previous state of the DO pin was digital logic high (bit 1), set it to low (bit 0), and vice versa, taking into account the current state of the DI signal latching into the DO pin.
8. Check the previous state of the DO signal at the clock's lowering edge. The output signal would remain unchanged until the next rising edge at the SCK pin is detected, regardless of the state of the DI signal.

This aforementioned algorithm was applied on the developed program to obtain a specified output functionality of the Attiny85 IC, such that the DO signal changed from digital logic low to high and vice versa on the rising edge of the clock signal on the SCK pin, depending on the state of the DI pin. In addition, the output signal at the DO pin remained unchanged until the next rising edge of the clock pulse detected at the SCK pin.

3.2. Accelerated aging methodology

The accelerated aging stress time-dependent experimental test setup is similar to that in [22,24], as depicted in Fig. 1, in order to implement the designed constant stress ADTs plan on the selected programmed IC samples (i.e., AT1–AT24) for a total stress duration T of 1000 h. Those fresh sample ICs were subjected to two different DC electrical voltage aging stress levels (i.e., 4 and 5 V) applied into the V_{cc} (pin 8) using the high temperature thermal resistant aging cables. Similarly, the remaining 12 fresh DUTs samples (i.e., AT13–AT24) were aged simultaneously according to the designed constant stress ADT plan presented in Table 1. Those constant multiple stress aging conditions were

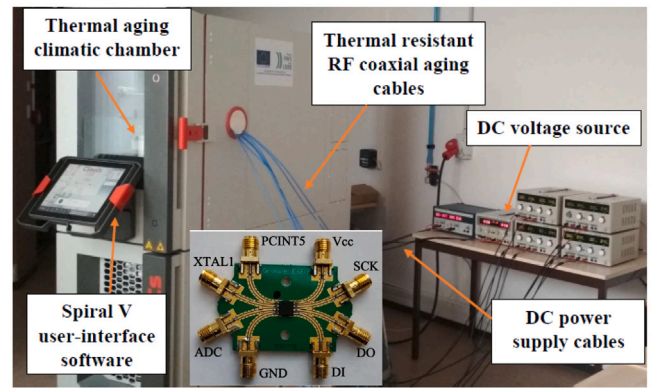


Fig. 1. Experimental test bench setup to perform the ADT plan.

applied simultaneously on all the fresh DUTs for ensuring permanent intrinsic degradation due to activating and accelerating the relevant failure mechanisms inducing the relevant failure mechanisms (i.e., hot carrier injection (HCI) and negative-bias transistor instability (NBTI)).

The evolution of the long-term electromagnetic robustness (EMR) of the ICs, depending on the applied aging stress magnitude and time duration, was investigated by implementing the repetitive method of applying the "Stress-Measurement-Stress" technique till the completion of the intended ADT plan, as shown in Table 1. The experimental methodology employed to characterize the long-term EMR variation with applied aging stress time intervals is similar to that of discussed in [22,24]. However, this methodological approach required pausing the accelerated aging process every 200 h stress duration, removing all the tested IC samples from the climatic chamber, and performing the DPI conducted immunity tests in nominal conditions (i.e., 25 °C and 3 V) on all the fresh and aged ICs, in order to assess and analyze the accelerated aging effect on the measured EMC performance variation at different stress times. Prior to resuming the accelerated aging process, the aged DUTs were placed to the climatic chamber. Therefore, the cycle was repeated after every 200 h of fixed aging stress duration for a total stress duration of 1000 h.

3.3. Conducted immunity test and measurement procedures

The conducted EMC performance of the tested ICs was evaluated by performing the non-destructive DPI test in accordance with the IEC 62132-4 standard [25]. The DPI test measurement test bench setup used for is similar to that discussed in [26] for performing the conducted immunity measurement on both the fresh and aged microcontroller IC samples. However, characterizing the EMC performance analysis of these aged Attiny85 IC samples required injecting the square-wave clock pulse into the SCK (pin 7) and the digital input signal into the DI (pin 5), varying between the nominal logic low voltage (V_L) level (i.e., 0.3 V) and the high voltage (V_H) level (i.e., 2.8 V) is illustrated in Fig. 2.

The conducted immunity measurement test apparatus for performing the DPI test on both fresh and aged microcontroller IC samples is depicted in Fig. 2. The test bench setup was utilized to characterize the conducted immunity parameters, which include measuring power injected (P_{inj}) at each corresponding DPI frequency (f) values by the direct coupling of the continuous-wave on the V_{cc} pin 8 to induce the DPI failure on the tested ICs. The measurement procedures involved to implement the DPI algorithm for evaluating the conducted immunity performance of both fresh and aged microcontroller IC samples is similar to that discussed in [26,27]. To define the DPI immunity threshold criterion, the digital circuit was considered to fail, while characterizing the EMC conducted immunity performance of those DUT samples, if the following perturbations criteria specified as follows would occur.

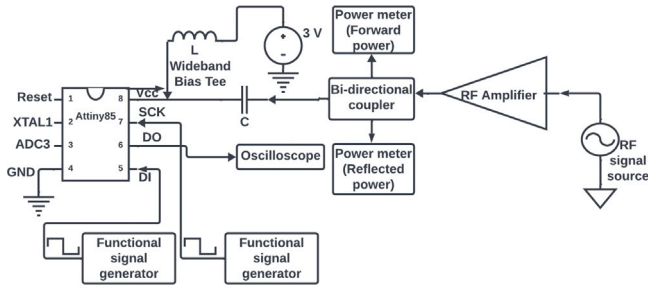


Fig. 2. Measurement test setup to evaluate the conducted immunity.

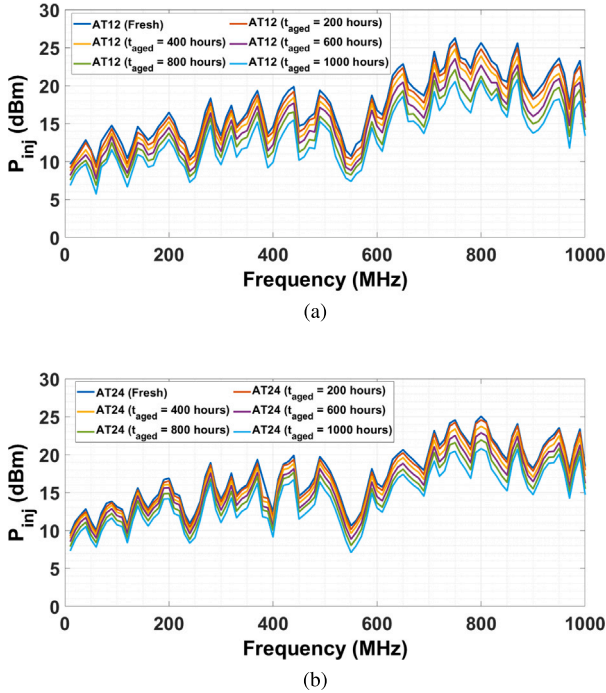


Fig. 3. Evolution of the conducted immunity level of Attiny85 samples at various aging stress duration caused by the identical 5 V electrical voltage stress and constant (a) high; (b) low thermal stress conditions.

1. either the low logic V_L or high V_H level of the DO signal exceeds the $\pm 10\%$ boundary limit, resulting in the positive or negative failure mode due to the RF signal injection into the V_{cc} pin.
2. either the timing variation observed at the rising or falling edges of the expected DO signal due to the noise induced by the EMI should not exceed the 10% limit. This phenomenon could be observed in the DO signal due to the noise induced to V_{cc} at the pin 8 of the IC, affecting its signal integrity and causing significant implication in its functional performance.

4. EMC performance evaluation of the DUTs: Results and analysis

The IC samples, namely AT6, AT12, AT18, and AT24, were subjected to different combinations of accelerated aging stress conditions, as outlined in Table 1. The conducted immunity performance degradation of these tested IC samples were compared and analyzed at different stress time intervals under the influence of both the applied thermal and electrical voltage stress factors.

Fig. 3 illustrates the EMC performance evolution of the tested fresh and aged AT12 and AT24 IC sample observed at different aging stress t_{aged} duration, subjected to the same electrical voltage (i.e., 5 V) stress levels but different thermal stress conditions (i.e., 110 °C and 70 °C).

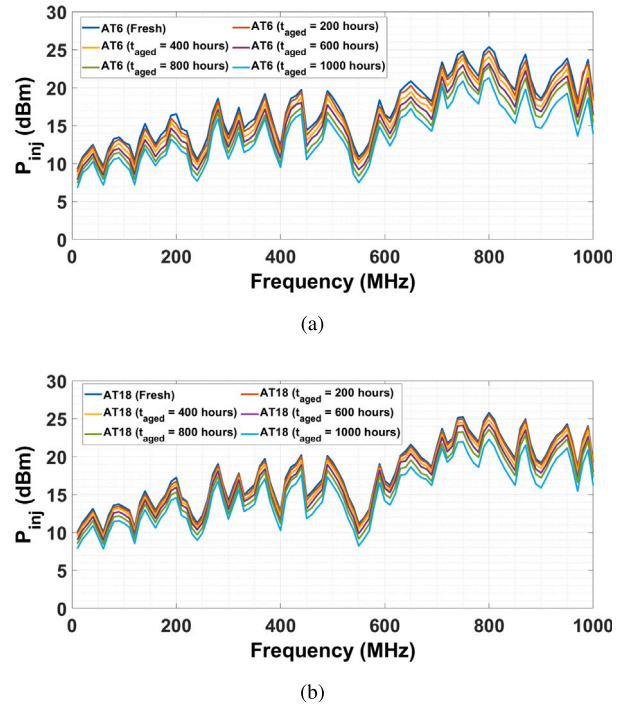


Fig. 4. Evolution of the conducted immunity level of Attiny85 samples at various aging stress duration caused by the identical 4 V electrical voltage stress and constant (a) high; (b) low thermal stress conditions.

Considering an increase of the t_{aged} intervals, the EMC performance of the tested IC samples, characterized by both the high and low immunity points, degraded at each corresponding frequencies varying between 10 and 1000 MHz, as shown in both Figs. 3(a) and 3(b). Although the P_{inj} was found to be comparable for the AT24 and AT12 ICs, Fig. 3(a) shows that the P_{inj} of the fresh AT12 decreased from 18.4 dBm to 13.3 dBm between 10 MHz and 1000 MHz. Consequently, Fig. 3(b) displays a smaller reduction of P_{inj} from 18.4 dBm to 14.7 dBm across the same tested DPI frequency range, after the completion of the total aging t_{aged} of 1000 h. Thus, the AT24 was found to be more immune compared to the AT12 over the entire ADT's stress duration due to applying 40 °C higher temperature stress.

The similar evolution of the EMC characteristics was also observed for both tested AT6 and AT18 IC samples in the Fig. 4. However, both the tested AT6 and AT18 samples demonstrated little impact on the conducted immunity degradation compared to those DUTs sample's (i.e., AT12 and AT24) conducted immunity performance evaluated across the entire DPI frequency range at different stress t_{aged} duration, as demonstrated in Figs. 4(a) and 4(b), respectively. This is because both AT6 and AT18 were subjected to a 7.3% lower electrical voltage stress magnitude compared to those AT12 and AT24 IC DUT samples, respectively, while the aging impact due to thermal stress remained identical. It is noteworthy to mention that the similar EMC performance was also obtained for the remaining 20 IC samples tested based on the defined constant stress ADT plan; results are not provided for the sake of brevity.

The effect of applying constant multiple stress factors (i.e., temperature and electrical voltage) on the EMC fluctuation of the recorded P_{inj} level between the fresh sample and the aged state at different aging t_{aged} duration was analyzed by computing the absolute power injected drift ($|\Delta P_{inj}|$) at each DPI frequency values between 10 and 1000 MHz. Figs. 5 and 6 compare the variation of the extracted absolute mean $|\Delta P_{inj}|$ degradation data computed as a function of tested frequency at different aging t_{aged} intervals. At different t_{aged} intervals, a significant decrease in the EMC performance of all tested ICs was observed due

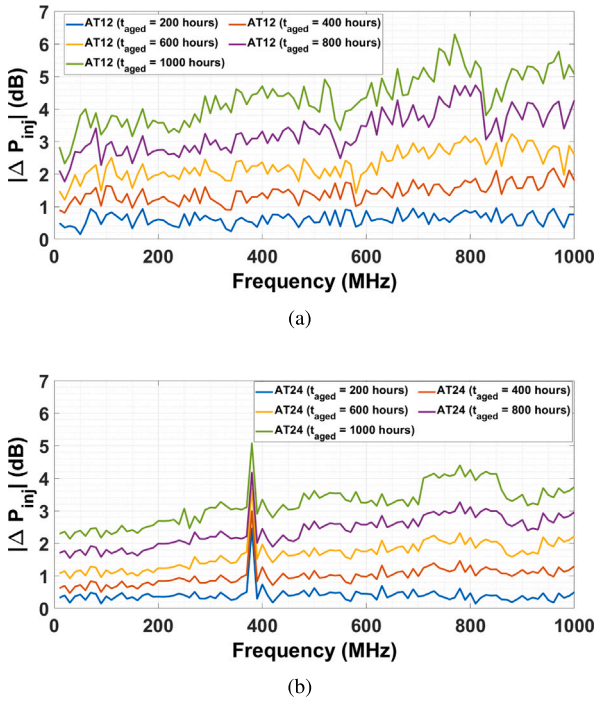


Fig. 5. Conducted immunity level drift of Attiny85 samples at various aging stress time caused by the identical 5 V electrical voltage stress as well as constant (a) high; and (b) low thermal stress conditions.

to the negative (positive) statistical computation of the $|\Delta P_{inj}|$ data extracted for each corresponding DPI frequency values by subtracting the measured P_{inj} of the fresh IC samples from that of the aged state. Notably, the remaining DUT samples exhibited a similar trend in the degradation of conducted immunity as characterized by evaluating the $|\Delta P_{inj}|$ across the entire tested DPI frequency range. Consequently, those results have not been included for the sake of brevity.

The observed increasing degradation of the conducted immunity level drift, characterized by evaluating the $|\Delta P_{inj}|$ corresponding to each tested DPI frequencies, was found to be reproducible which could be due to the increasing failure rate of the accelerated intrinsic failure mechanisms (i.e., HCI and NBTI) induced by applying multiple accelerated aging stress conditions. These failure mechanisms could potentially change the intrinsic parameters of the internal transistors of the digital circuit within the tested Attiny85 IC samples, increasing the threshold voltage (V_{th}) and reducing the effective charge carrier (i.e., electrons and holes) mobility (μ_{eff}) of those aged internal NMOS and PMOS transistors [28,29]. Moreover, these induced failure mechanisms may apply large drain–source voltage (V_{ds}) across the drain and source terminals of those aged internal CMOS transistors, causing a substantial reduction of drain–source current (I_{ds}) propagating through these two terminals [8,13].

The above aforementioned phenomenon could also be explained using the mathematical relationship between I_{ds} and V_{th} provided in [29]. Therefore, trans-conductance g_m parameter of the aged transistor could also be reduced proportionally. Finally, the switching speed of the aging internal transistors of the digital circuit embedded within the DUT could decrease, thereby increasing the propagation delay of the signal transmitting through the internal logic gates of the tested ICs [8,28]. Hence, an appropriate timing and clock synchronization between the DI and clock signal at the SCK pin could no longer be assured, leading in DO signal distortion and a deterioration in the conducted immunity performance of the aged DUT.

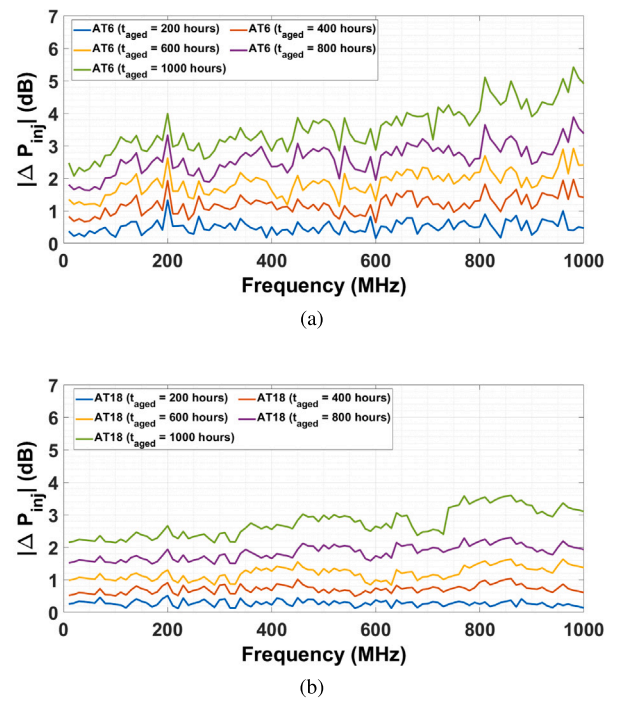


Fig. 6. Conducted immunity level drift of Attiny85 samples at various aging stress time caused by the identical 4 V electrical voltage stress as well as constant (a) high; and (b) low thermal stress conditions.

5. EMC performance degradation path modeling of the aged DUTs

This section compares the conducted immunity degradation of four different DUT samples (i.e., AT6, AT12, AT18 and AT24) under the influence of applying multiple accelerated aging conditions presented in Table 1, followed by providing a methodological approach to develop the degradation path model based on the observed EMC performance degradation. Those unknown degradation path model constants were estimated, along with determining the pseudo TTF data for those DUT samples based on the defined conducted immunity degradation criterion (D). Thus, parameter estimation of those generated EMC degradation paths, corresponding to various aging stress magnitudes, would allow for the prediction of the required EMC degradation data under any tested or untested environmental stress conditions.

5.1. Impact of ADTs on the conducted immunity of ICs

Fig. 7 illustrates an increasing conducted immunity performance curves for each of the tested IC samples (i.e., AT6, A12, AT18 and AT24), characterized by the mean $|\Delta P_{inj}|$ data plotted on the y-axis against the aging stress duration of time on the x-axis. Since the measured P_{inj} data of the tested DUTs was dependent on both the DPI frequency and aging stress duration, consequently the extracted $|\Delta P_{inj}|$ data also varied based on both the frequencies and aging stress t_{aged} duration. Hence, the average $|\Delta P_{inj}|$ was considered as a suitable parameter for representing the aging stress time-dependent evolution of the EMC performance degradation on the tested ICs. At each stress intervals of t_{aged} , the mean $|\Delta P_{inj}|$ was computed by taking the sum of all the $|\Delta P_{inj}|$ extracted for each corresponding tested DPI frequency followed by dividing the evaluated total $|\Delta P_{inj}|$ by the total number of the considered frequency values. This statistical computation of the absolute mean $|\Delta P_{inj}|$ is represented by a mathematical expression as shown in Eq. (1), where P_{injX_f} refers to the injected power after aging, P_{injY_f} denotes the power injected to the tested IC sample's V_{cc} pin 8 at each DPI frequencies before aging, f_a and f_b corresponds to

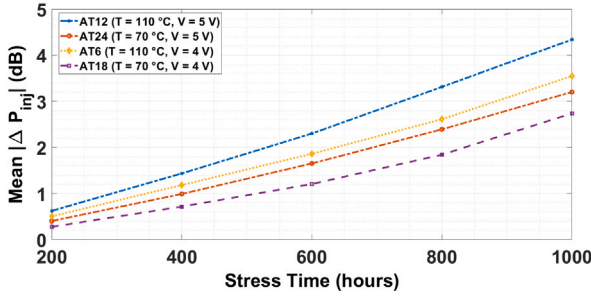


Fig. 7. Conducted immunity degradation as a function of stress time under the influence of accelerated aging conditions on the tested IC samples.

the minimum and maximum tested DPI frequency value respectively, varying between 10 and 1000 MHz with a step-size of 10 MHz between each frequency points, and $n_{frequency}$ is the total number of tested frequency values.

$$\overline{|\Delta P_{inj}|} = \frac{1}{n_{frequency}} \sum_{f=f_a}^{f_b} |P_{injX_f} - P_{injY_f}| \quad \text{for } f_a \leq f \leq f_b \quad (1)$$

Depending on the applied accelerated multiple stress conditions specified by the design of the constant stress ADT plan, Fig. 7 has also displayed a significant increment of the mean $|\Delta P_{inj}|$ with increasing stress duration for all the tested IC samples. The conducted immunity performance evolution of these tested IC samples could be compared by noticing significant difference in the mean $|\Delta P_{inj}|$ at various stress times. After the completion of the performed ADTs, the aged AT12 DUT showed the highest conducted immunity degradation, demonstrating a mean $|\Delta P_{inj}|$ of 4.3 dB over the whole frequency range, compared the rest of the tested IC samples. Under the influence of the identical thermal stress but different electrical stress level conditions, the aged AT6 sample showed a total of 22.3% lower immunity degradation compared to the aged AT12 DUT. In addition, as illustrated in Fig. 7, the AT24 sample IC aged at the low thermal (i.e., 70 °C) and high electrical voltage (i.e., 5 V) aging stress condition for 1000 h exhibited a 17.2% greater conducted immunity performance degradation compared to that of the aged AT18 sample DUT with the similar accelerated thermal stress and a lower electrical stress conditions.

5.2. Evolution of EMC degradation: Modeling and parameter estimation

Fig. 8 depicts the monotonic evolution of the monotonic degradation of the tested IC samples at different stress time over the whole tested DPI frequency range (i.e., 10–1000 MHz). For a fixed aging stress time measured in hours, both the computed $|\Delta P_{inj}|$ and the measured nominal P_{inj} data of the fresh DUTs before aging varied in each frequency points over the entire tested frequency range. The ratio of the $|\Delta P_{inj}|$ to that of the P_{inj} data was evaluated. The mean of the ratio for every frequency at various stress times, denoted by the parameter G was computed, which is expressed by the mathematical expression as shown in Eq. (2), where $|\Delta P_{inj}|$ is the computed power injected drift at each DPI tested frequency values and the P_{injY_f} is the power injected before aging at those corresponding frequencies at various stress times.

$$G = \frac{1}{n_{frequency}} \cdot \left[\sum_{f_a}^{f_b} \frac{|\Delta P_{inj}|}{P_{injY_f}} \right] \quad (2)$$

The deterioration of the conducted immunity performance of those tested IC samples increased with time at each frequency, as illustrated in Fig. 7. Thus, the parameter G was considered as the suitable aging stress t_{aged} dependent EMC degradation path modeling indicator parameter for the tested ICs, as illustrated in Fig. 8. It could be observed that the tested AT12 showed significantly higher mean G of 25.5%

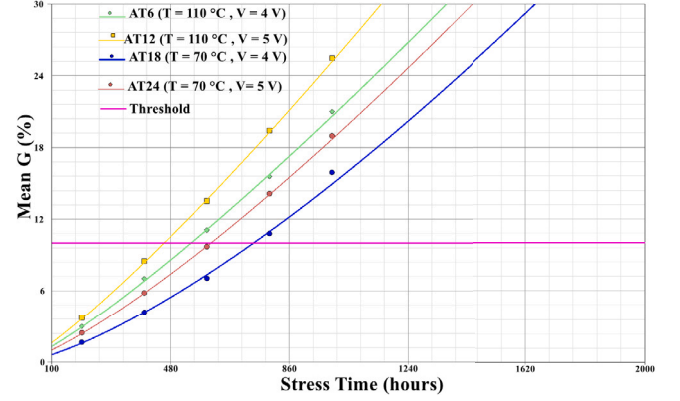


Fig. 8. Degradation paths fitted to the computed EMC degradation of the tested IC samples.

compared to that of 21% for the AT6 sample subjected to the identical T but 50% lower V stress level, after the completion of the total stress duration. Besides, similar increasing monotonic degradation trend over the total stress duration is observed for all those DUT samples subjected to different combinations of applied thermal (T) stress and electrical voltage (V) stress conditions. Those non-linear best-fit degradation paths were generated, which follows a suitable agreement with the computed mean G EMC degradation data points, as highlighted in Fig. 8. The choice of the proposed stress-dependent degradation path model, which considered the n th power MOSFET law model [30] to describe the degradation trend varying with stress time duration. Applying the regression analysis on the evolution of the measured EMC performance degradation data of the studied ICs, the correlation coefficient R^2 was obtained to characterize the goodness of the fit for the selected EMC degradation path model. The evaluated R^2 constant value was found to be closer to the maximum 1 for those studied IC samples as shown in Table 2, which implies the appropriateness of the model and the degree of accuracy to which the observed EMC degradation paths best-fits to the EMC performance degradation data, as exhibited in Fig. 8.

$$y_{ikl}(t) = A_{ikl} \cdot t^\gamma \quad (3)$$

$$\log(y_{ikl}(t)) = \log\left(\frac{\Delta P_{inj}}{P_{inj}}\right) = \log(A_{ikl}) + \gamma \log(t) \quad (4)$$

$$t_{failure} = \exp\left(\frac{\log(y_{ikl}(t)) - \log(A_{ikl})}{\gamma}\right) \quad (5)$$

The simplified mathematical expression to model those generated monotonic degradation paths at various stress duration and magnitudes is provided in Eq. (3), where $y_{ikl}(t)$ refers to the mean G (denoted by %), A and γ are the stress-dependent unknown model constants, i is the DUT sample unit, k refers to the V stress level and l is the T constant stress level. Applying the regression analysis on the developed model expressed in (3) allowed to estimate those relevant unknown model constants (i.e., A and γ). Determining the model constants would enable to predict the EMC degradation data based on the known values of stress duration for any tested or untested accelerated stress conditions. Non-destructive EMC degradation path modeling analysis was performed to determine the pseudo TTF data that could be determined both graphically and mathematically, depending on the user-defined failure threshold D criterion. A failure threshold D of 10% on the observed EMC degradation data is shown by the horizontal line (purple) in Fig. 8. Applying the logarithm on both sides of Eq. (3), such that the $y_{ikl}(t)$ is referred to logarithmic mean ratio of the variation of $|\Delta P_{inj}|$ from that of the nominal P_{inj} before aging of the tested IC as shown in Eq. (4). The mathematical expression for determining the pseudo

Table 2

EMC degradation path modeling parameters and TTF data of various tested IC samples.

| IC references | Parameters | | | |
|---------------|------------|----------|----------------|-------------|
| | A | γ | R ² | TTF/(hours) |
| AT6 | 0.0052 | 1.1988 | 0.9996 | 549 |
| AT12 | 0.0072 | 1.1593 | 0.9998 | 514 |
| AT18 | 0.0011 | 1.3801 | 0.9976 | 739 |
| AT24 | 0.0029 | 1.2683 | 0.9999 | 616 |

TTF data is represented as the estimated failure time $t_{failure}$, based on the considered degradation over the stress time, is provided in (5), using the predicted values of the model constants A and γ .

Table 2 shows the model parameters and the computed TTF data of IC samples tested at multiple constant multiple stress factors with different stress magnitude. It is worth mentioning that this developed degradation path model was employed for the rest of the samples for determining their corresponding $t_{failure}$ and other relevant model parameters. It is observed that these estimated model parameters varied for different tested IC samples, depending on the choice of the aging stress-dependent factors (i.e., T , V , t_{aged} and T stress duration), thus contributing to the significant EMC degradation at various acceleration factors due to T and V aging stress levels.

6. ALT modeling and reliability analysis of the DUTs

This section deals with highlighting the ALT modeling methodology by taking into account of the combined overall contribution of both T and V constant stress conditions on the life-stress distribution data, highlighting an acceptable accuracy of the developed predictive reliability model to predict the conducted immunity lifetime reliability estimation metrics (i.e., failure probability, model constants) with corresponding pseudo TTF data of each of the DUT sample ICs in nominal condition.

6.1. Life-stress model of the aged IC samples

Considering the Weibull reliability function $R(t)$ express as shown in (6) with η and β refers to the scale and shape, respectively [31].

$$R(t) = e^{-\left(\frac{t}{\eta}\right)^\beta} \quad (6)$$

Hence, the two parameters Weibull probability density function (PDF) expression can be derived as provided in (7).

$$f(t) = \frac{\beta}{\eta} \left(\frac{t}{\eta}\right)^{\beta-1} \cdot e^{-\left(\frac{t}{\eta}\right)^\beta} \quad (7)$$

Since both the temperature T and voltage V stress factors were applied simultaneously on the selected DUT samples that resulted to obtain the EMC performance degradation data, the generalized Eyring-ALT model was considered to demonstrate the analytical relationship between the quantifiable lifetime (L) and those combined impact of both T and V constant stress levels in (8), where the $L(T, V)$ refers to the life-data relationship with the applied T and V stress factors on the tested IC samples, unknown model constants (i.e., A , B , C and D) depends on sample design and properties that was estimated by combining this model with the two-parameter Weibull distribution and applying the maximum likelihood estimation (MLE) method to estimate those unknown model parameter. Unlike the simplified Eyring-ALT model that takes into account of the impact of T stress only on the lifetime L of a tested sample, the developed mathematical life-stress model is an extension of the simplified Eyring-ALT model.

$$L(T, V) = \frac{1}{T} \cdot \exp(A) \cdot \exp\left(\frac{B}{T}\right) \cdot \exp(CV) \cdot \exp\left(\frac{DV}{T}\right) \quad (8)$$

Table 3

ALT reliability modeling parameters for the tested IC samples.

| Model parameters | Data |
|------------------|---------|
| A | 9.24 |
| B | 1327.86 |
| C | 0.30 |
| D | -155.41 |
| L_f | -106.09 |
| β_w | 32.68 |
| η | 1507.44 |

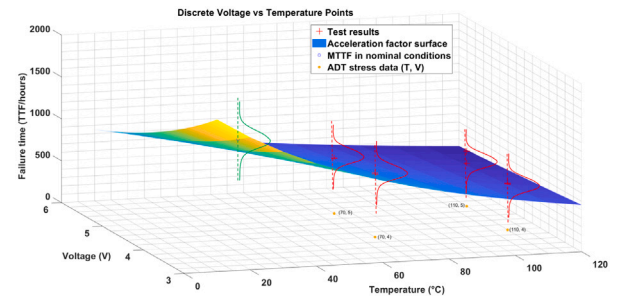


Fig. 9. Weibull distribution model parameter distribution at each combinations of applying both constant thermal and electrical voltage stress magnitude.

The model takes into account of any strong interaction between the thermal T and non-thermal (i.e., electrical voltage) stress factors using the last exponential term using the model constant $\left(\frac{DV}{T}\right)$ term as shown in (8), allowing to predict the effect of varying one of the individual stress factors on the lifetime L stress data is dependent on the stress level of the other stress factor. In the other words, it can also be implied that the impact caused by the acceleration factor due to the T would depend on the stress magnitude of the V stress and vice versa [31,32]. The generalized Eyring-Weibull PDF expression can be obtained by substituting the (9) in (7), where the scale η is equivalent to the $L(T, V)$ as shown in (9).

$$\frac{1}{\eta} = L(T, V) = T \cdot \left[\exp(A) \cdot \exp\left(\frac{B}{T}\right) \cdot \exp(CV) \cdot \exp\left(\frac{DV}{T}\right) \right] \quad (9)$$

Thus, the mathematical expression for the combined generalized-Weibull two parameters Weibull probability density function (PDF) is denoted by $f_w(t, T, V)$ as shown in (10). Overall, the derived mathematical expression for the developed life-stress reliability model denoted by $R(t, T, V)$ is expressed in (11).

$$f_w(t, T, V) = \frac{\beta_w}{L(T, V)} \left(\frac{1}{L(T, V)} \cdot t^{\beta_w-1} \right) \cdot \exp\left(-\frac{t}{L(T, V)}\right)^{\beta_w} \quad (10)$$

$$R(t, T, V) = \exp\left[-\left(t \cdot T \exp\left(-A + \frac{B}{T}\right) \exp\left(CV + \frac{DV}{T}\right)\right)^{\beta_w}\right] \quad (11)$$

$$\ln(L_f(t)) = \sum_{l=1}^2 \sum_{k=1}^2 \sum_{i=1}^{n_k} \ln(f_{ikl}(t_i)) \quad (12)$$

Applying the MLE method along with the minimum function optimization technique using Eq. (12), taking into account of the $t_{failure}$ data of those tested IC samples, allowed to obtain unknown ALT reliability model constants and Weibull distribution parameters β_w and η , which are provided in Table 3. Fig. 9 illustrates the distribution of model parameter estimation at each of the four different stress (i.e., T and V) magnitudes. It also demonstrates the distribution of the computed TTF data points for the tested IC samples along the acceleration factor surface caused by various multiple accelerated aging stress conditions as well as the mean time-to-failure (MTTF) data in nominal condition.

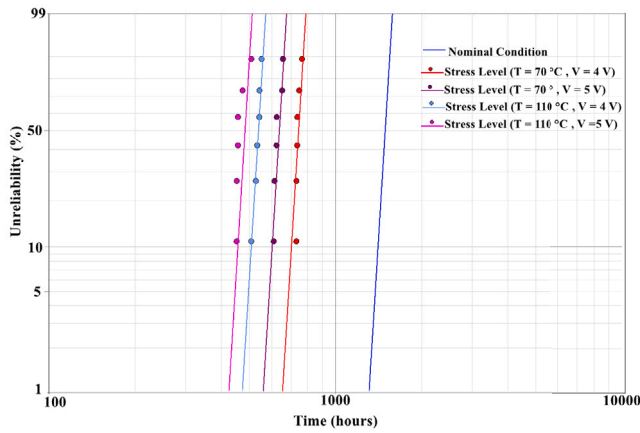


Fig. 10. Lifetime unreliability distribution of the logarithmic fits to the pseudo TTF data for each tested IC samples at different accelerated stress conditions.

6.2. Lifetime reliability modeling analysis of DUTs

The developed generalized Eyring–Weibull life-stress relationship was employed to characterize lifetime reliability model parameters depending on the conducted immunity performance characteristics of the tested IC samples caused by different multiple combinations of constant stress magnitudes for a fixed stress duration. Fig. 10 illustrates a set of parallel lines, produced by applying the Weibull distribution on the developed reliability model, which fits to the computed pseudo TTF data for each DUT samples. Those sets of parallel lines is a representation of the predicted unreliability, which corresponds to the combined influence of both thermal and electrical voltage stress factors with different stress magnitudes. In addition, those pseudo TTF data points evaluated based on the defined failure threshold considered on the observed EMC degradation data. The developed model could predict the unreliability (or failure probability) for all those selected tested IC samples with a very acceptable accuracy as insignificant difference between the Weibull distribution plots of the unreliability function and those computed TTF data points is depicted in Fig. 10.

Fig. 10 exhibits the EM unreliability (expressed in percentile) for all the six selected DUT samples tested at different combinations of accelerated aging stress conditions above the nominal conditions (i.e., 25 °C and 3 V). The unreliability of all the tested 24 samples, depending on the EMC performance degradation, shows a linear increasing trend, varying from 10% to 90% on the y-axis against the increasing pseudo TTF data points (between 450 and 850 h, respectively) on the x-axis. The tested AT12 sample DUT, under the combined impact of multiple stress factors at the constant stress magnitude of 110 °C and 5 V, showed the least pseudo TTF (514 h with 90% unreliability) compared to the AT24 (616 h with 10% unreliability) sample aged at 70 °C and 5 V. Likewise, the AT6 sample aged at 4 V and 110 °C took 549 h to fail with 90% unreliability, while the AT18 sample survived for 749 h prior to reaching the similar failure probability. Similarly, the effect of applying different electrical voltage V stress levels alone on the lifespan reliability of the tested ICs while keeping the same magnitude of temperature stress was also observed in Fig. 10.

While comparing the pseudo TTF data between the AT6 and AT12 samples, it can be observed that the failure time data for those two DUT samples differed by 35 h for reaching the maximum 90% unreliability. On the other hand, both the tested AT18 and AT24 samples, aged at a similar lower thermal stress (i.e., 70 °C) compared to that of the other two selected tested samples, took longer pseudo TTF based on the observed EMC degradation data. Comparing the unreliability of two samples, it is observed that the AT18 sample demonstrates a higher level of unreliability. Specifically, the AT18 sample exhibits a survival time of around 739 h until it reaches a 90% failure probability

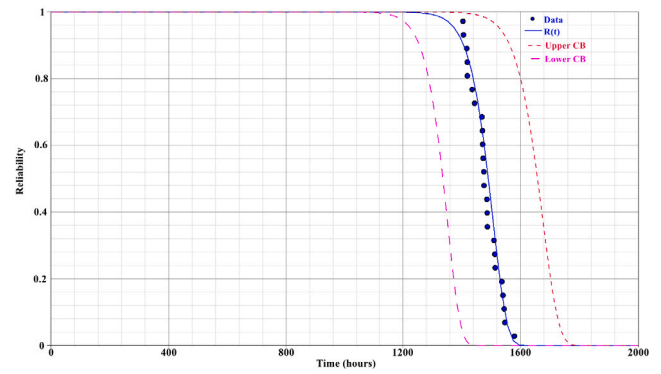


Fig. 11. Conducted immunity reliability function curve fits to the estimated lifetime data of the tested IC samples within the confidence interval based on the developed ALT EM reliability model.

compared to the AT24 sample, with a lower level of reliability (10% unreliability at approximately 649 h). Therefore, based on the assessed immunity performance of the evaluated IC samples, it can be deduced that the least amount of unreliability results from simultaneously applying the lowest magnitudes of thermal and electrical voltage stress factors to the chosen DUT samples. This would enable the IC samples to endure for an extended duration. Moreover, the developed reliability model also allows to predict the failure time of these DUT samples in nominal condition, as shown in Fig. 10. It is also observed that the proposed reliability model would plot the predicted unreliability in nominal condition, implying that all those tested samples predicted lifetime would be between 1100 and 1600 h.

Considering the soft failure 10% failure threshold D criterion on the measured test data in accelerated aging conditions, Fig. 11 displays the estimated EMC end-of-life model data points associated with each reliability or survival probability data in nominal condition, which was obtained by applying the extrapolation technique to the developed ALT reliability model. It illustrates that the TTF model data best fits the conducted immunity EM reliability function curve in nominal conditions. Those predicted immunity pseudo TTF model data points on the x-axis correspond to the survival probability on the y-axis for each of the tested IC DUT samples. These estimated lifetime EMC reliability model points lies within both the upper and lower confidence bounds (CB) curves (ranging between the 10% and 90% confidence intervals) at the 80% confidence level, validating the accuracy of the developed model and indicating the uncertainty that can be found within the acceptable range of the model prediction. Based on the considered user-defined EMC failure threshold D criterion, it is also worth mentioning that the estimated TTF data points in nominal condition was found to be higher with lower probability of failure than that of the computed EMC pseudo TTF data points of the tested IC samples subjected to aged accelerating aging stress conditions.

Fig. 11 demonstrates the conducted immunity lifetime reliability function curve that best fits to the estimated lifetime data of all the DUT samples in nominal condition. The non-linear decreasing trend of the EM immunity lifetime reliability function curve implies that the predicted non-failure or survival probability of the considered DUT samples operating in nominal condition would decrease with an increasing of operational time. The reliability function $R(t)$ corresponding to this curve is derived from the developed reliability model, and can be expressed using the mathematical expression provided in (11).

Fig. 11 exhibits the EMC reliability (or non-failure probability) on the y-axis remained 1.0 till 1200 h, thereby implying all the 24 selected IC samples would survive in nominal condition until this time period. In addition, all 24 data points that correspond to the predicted lifetime reliability parameters were plotted on the x-axis against the reliability and/or survival probability values on the y-axis. The EM

immunity reliability function curve predicts that the AT12 would fail at around 1150 h with the 10% survival probability. On the other hand, a predicted lifetime reliability of 90% reliability would be observed for the AT24 sample that would fail at around 1350 h. Thus, it is observed that all the 24 DUT samples would fail beyond the total applied accelerated stress duration, which corresponds to a very high form factor identified in Table 3. This implies that the failure mode and the *TTF* are highly deterministic, indicating a specific physics of failure mechanisms in time. Overall, the developed ALT reliability model demonstrated satisfactory accuracy in estimating the EMC failure probability of the model data points associated with the tested IC samples. This was achieved by utilizing the immunity degradation measurement data acquired through the designed ADT's implementation for a total specified stress duration. It can be deduced that those examined samples would fail after a more prolonged period of time, as indicated by a reduced predicted lifetime reliability.

The developed predictive EM reliability model, which is based on the assessed conducted immunity of the tested digital ICs, provides useful insights associated with the lifetime reliability with regards to the EMC compliance of electronic IC components during the design phase of the digital ICs and/or electronic components. As a result, by employing the reliability model function of environmental constraints, IC designers would be able to implement EMC protection measures and optimize the internal circuit design of such electronic IC devices in order to improve their lifetime reliability for nominal operational conditions. Furthermore, an accurate estimation of the constructed degradation and reliability model's parameters would enable forecasting the long-term EM robustness to EM interference and the expected EMC failure and/or non-failure probability in both normal and untested environmental stress conditions.

Regarding the limitations associated with such a developed EM lifetime reliability model, it has been constructed from adequate samples of identical IC with similar internal circuits and layouts designed in the same CMOS technology and production batch, in order to avoid any manufacturing contingencies. Consequently, an immediate transposition of the model to another integrated circuit would not be possible. Thus, an ADT plan needs to be designed and implemented to construct the data-driven degradation and reliability model. Random effects caused by the influence of aging stress on the EMC performance degradation behavior of those DUT samples, as well as measuring equipment variability, might potentially account for the observed dispersion of conducted immunity measurement data. As a result, the randomness of the conducted immunity measurement data from the tested samples could likely be challenging to compute pseudo *TTF* and other essential reliability metrics of the created model with an acceptable degree of accuracy under various aging constraints.

7. Conclusion

The study showed the predicted lifetime reliability modeling and analysis of the chosen Attiny85 microcontroller DUT samples, based on the EMC performance degradation when multiple accelerated aging constraints. The integration of the generalized Eyring life-stress ALT model and the Weibull distribution allowed the construction of a predictive reliability model that demonstrated acceptable accuracy when applied to *TTF* data points computed statistically. Analyzing the produced lifetime reliability model as a function of conducted immunity performance revealed that the EM unreliability (or failure probability) varied between 10% and 90% for all the tested IC samples, irrespective of applying various combinations of constant *T* and *V* aging stress conditions. Among all those tested ICs, AT6–AT12 (i.e., 6 units) samples, aged at the highest *T* and *V* stress magnitude, exhibited the least pseudo *TTF* data compared to those IC samples, which were tested with the least *T* and *V* aging stress magnitudes (i.e., AT13–AT18), when a fixed user-defined 10% failure *D* criterion was considered on the EMC performance degradation data.

Moreover, it was demonstrated that altering the magnitude of the applied *V* stress had a substantial effect on the DUTs while keeping the *T* stress constant. Consequently, the survival probability predictions for all DUT IC samples under nominal conditions exhibited a declining trend in the function curve of the devised reliability model, which was derived based on the conducted EMC performance degradation caused by implementation of the ADT plan. Thus, the IC samples evaluated under the most severe aging stress circumstances exhibited the least *TTF* with the highest failure probability.

Overall, the developed physics-based reliability modeling approach was able to produce an accurate estimation of the developed generalized Eyring ALT model combined with the Weibull statistical distribution, in order to assess the lifetime reliability metrics with an acceptable level of accuracy and precision for any defined or undefined multiple combinations of both *T* and *V* constant stress levels. Concerning the Weibull distribution, a very high form factor is identified, implying that the failure mode and hence the *TTF* are highly deterministic and should be further investigated regarding the physics of failure.

CRedit authorship contribution statement

Jaber Al Rashid: Conceptualization, Methodology, Data curation, Formal analysis, Writing – original draft. **Mohsen Koohestani:** Validation, Visualization, Writing – review & editing. **Laurent Saintis:** Software, Validation, Writing – review & editing, Funding acquisition. **Mihaela Barreau:** Supervision, Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

Acknowledgments

This work is carried out in the framework of a PhD thesis in collaboration between the LARIS laboratory of the “University of Angers” and the “ESEO School of Engineering”. This research is co-financed by the Région Pays de la Loire and the University of Angers.

References

- [1] F. Wan, J. Ge, Ge, Y. Zhou, B. Yu, Improved immunity measurement of a microcontroller to conducted continuous wave interference, *Prog. Electromagn. Res. M* 31 (2013) 117–127, <http://dx.doi.org/10.2528/PIERM13041902>.
- [2] M. Amellal, S. Op't Land, R. Perdriau, M. Ramdani, A. Ahaitouf, M. Drissi, Direct power injection on functional and non-functional signals of SPI EEPROM memories, in: 10th International Workshop on the Electromagnetic Compatibility of Integrated Circuits, EMC Compo, 2015, pp. 24–28, <http://dx.doi.org/10.1109/EMCCompo.2015.7358324>, Nov. 10–13, 2015.
- [3] T. Su, T. Steinecke, M. Unger, Origins of electromagnetic immunity holes of microcontrollers, in: 2010 IEEE Electrical Design of Advanced Package and Systems Symposium, 2010, pp. 1–4, <http://dx.doi.org/10.1109/EDAPS.2010.5683027>.
- [4] A. Alaeldine, J. Cordi, R. Perdriau, M. Ramdani, J.L. Levant, Predicting the immunity of integrated circuits through measurement methods and simulation models, in: 2007 18th International Zurich Symposium on Electromagnetic Compatibility, EMC Europe, 2007, pp. 79–82, <http://dx.doi.org/10.1109/EMCZUR.2007.4388200>.
- [5] J. Wu, C. Li, B. Li, W. Zhu, H. Wang, Microcontroller susceptibility variations to EFT burst during accelerated aging, *Microelectron. Reliab.* 64 (2016) 210–214, <http://dx.doi.org/10.1016/j.microrel.2016.07.099>.
- [6] Q.M. Khan, M. Koohestani, M. Ramdani, R. Perdriau, Obsolescence in EMC risk assessment: A case study on EFT immunity of microcontrollers, in: 2020 International Symposium on Electromagnetic Compatibility, EMC Europe, Krakow, Poland, 2020, pp. 1–6, <http://dx.doi.org/10.1109/EMCEUROPE48519.2020.9245783>.

- [7] J. Rashid, M. Koohestani, L. Saintis, M. Barreau, A state-of-the-art review on IC reliability, in: Proceedings of the 31st European Safety and Reliability Conference, ESREL, Angers, France, 2021, pp. 1850–1857, <https://hal.univ-angers.fr/hal-03361394>.
- [8] A. Boyer, S.B. Dhia, B. Li, N. Berbel, R. Fernandez-Garcia, Experimental investigations into the effects of electrical stress on electromagnetic emission from integrated circuits, *IEEE Trans. Electromagn. Compat.* 56 (1) (2013) 44–50, <http://dx.doi.org/10.1109/TEMC.2013.2272195>.
- [9] A. Boyer, S. Ben Dhia, Characterization and modeling of electrical stresses on digital integrated circuits power integrity and conducted emission, in: 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits, EMC Compo, 2013, <http://dx.doi.org/10.1109/EMCCompo.2013.6735199>.
- [10] W.Q. Meeker, L.A. Escobar, F.G. Pascual, *Statistical Methods for Reliability Data*, John Wiley & Sons, 2022.
- [11] W.Q. Meeker, L.A. Escobar, A review of recent research and current issues in accelerated testing, *Int. Stat. Rev./Rev. Int. Stat.* 61 (1) (1993) 147–168, <http://dx.doi.org/10.2307/1403600>.
- [12] N. Gorjian, L. Ma, M. Mittinty, P. Yarlagadda, Y. Sun, A review on degradation models in reliability analysis, in: *Engineering Asset Lifecycle Management*, Springer, London, 2010, pp. 369–384, <http://dx.doi.org/10.1007/978-0-85729-320-6-42>.
- [13] B. Khaleghi, T. Rosing, Reliability Degradation in Nanoscale CMOS: A Review of Modeling, Monitoring, and Mitigation Techniques, ResearchGate, 2019, pp. 1–23, <http://dx.doi.org/10.13140/RG.2.2.32420.42883>.
- [14] L.A. Escobar, W.Q. Meeker, A review of accelerated test models, *Statist. Sci.* 21 (4) (2006) 552–577, <http://dx.doi.org/10.1214/088342306000000321>.
- [15] B. Zheng, et al., Reliability estimation of complex systems based on a Wiener process with random effects and D-vine copulas, *Microelectron. Reliab.* 138 (2022) <http://dx.doi.org/10.1016/j.microrel.2022.114640>.
- [16] S. Zhao, S. Chen, H. Wang, Degradation modeling for reliability estimation of DC film capacitors subject to humidity acceleration, *Microelectron. Reliab.* 100–101 (2019) <http://dx.doi.org/10.1016/j.microrel.2019.113401>.
- [17] H. Liu, C. An, W. Zhang, Z. Dou, X. Tong, Life prediction of power devices of VIENNA rectifier considering the effects of aging and dust accumulation, *Microelectron. Reliab.* 138 (2022) (2022) <http://dx.doi.org/10.1016/j.microrel.2022.114723>.
- [18] I. Marzou, et al., Reliability assessment of miniaturised electromechanical RF relays for space applications, *Microelectron. Reliab.* 138 (2022) <http://dx.doi.org/10.1016/j.microrel.2022.114753>.
- [19] S. Chakraborty, et al., Reliability assessment of a WBG-based interleaved bidirectional HV dc/DC converter for electric vehicle drivetrains, in: 2020 Fifteenth International Conference on Ecological Vehicles and Renewable Energies, EVER, 2020, pp. 1–8, <http://dx.doi.org/10.1109/EVER48776.2020.9243021>.
- [20] C. Ghfiri, A. Boyer, A. Bensoussan, A. Durier, Ben Dhia, A new methodology for EMC prediction of integrated circuits after ageing, *IEEE Trans. Electromagn. Compat.* 61 (2) (2019) 572–581.
- [21] J. Al Rashid, L. Saintis, M. Koohestani, M. Barreau, Coupling simulation and accelerated degradation model for reliability estimation: application to a voltage regulator, *Microelectron. Reliab.* 138 (2022) <http://dx.doi.org/10.1016/j.microrel.2022.114682>.
- [22] J. Al Rashid, M. Koohestani, L. Saintis, M. Barreau, J. Al Rashid, M. Koohestani, L. Saintis, M. Barreau, Degradation and Reliability Modeling of EM robustness of voltage regulators based on ADT: An approach and a case study, *IEEE Trans. Dev. Mater. Reliable* 177–189 (2023) <http://dx.doi.org/10.1109/TDMR.2023.3340426>, (Early Access).
- [23] Atmel 8-bit Attiny85V-20PU, Farnell, 2024, [Online], Available: <https://fr.farnell.com/microchip/attiny85-20pu/mcu-8bit-attiny-20mhz-dip-8/dp/1455162>. (Accessed 04 March 2024).
- [24] J. Al Rashid, M. Koohestani, L. Saintis, M. Barreau, High temperature accelerated ageing influence on the conducted immunity modelling of the commonly used voltage regulator ICs, in: International Symposium and Exhibition on Electromagnetic Compatibility, EMC Europe, 2023, <http://dx.doi.org/10.1109/EMCEurope57790.2023.10274315>.
- [25] *Integrated Circuits-Measurement of Electromagnetic Immunity 150 KHz To 1 GHz-Part 4: Direct RF Power Injection Method*, IEC 62132-4, first ed., 2006.
- [26] J. Al Rashid, M. Koohestani, R. Perdriau, L. Saintis, M. Barreau, Combining obsolescence and temperature stress to evaluate the immunity of voltage regulators to direct power injection in long lifespan systems, *IEEE Lett. Electromagn. Compat. Pract. Appl.* 5 (1) (2023) 27–32, <http://dx.doi.org/10.1109/LEMCPA.2023.3240621>.
- [27] I. Chahine, M. Kadi, E. Gaboriaud, A.A. Louis, B. Mazari, Characterization and modeling of the susceptibility of integrated circuits to conducted electromagnetic disturbances up to 1 GHz, *IEEE Trans. Electromagn. Compat.* 50 (2) (2008) 285–293, <http://dx.doi.org/10.1109/TEMC.2008.918983>.
- [28] S.B. Dhia, A. Boyer, Electro-magnetic robustness of integrated circuits: from statement to prediction, in: 2013 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits, EMC Compo, 2013, pp. 208–213, <http://dx.doi.org/10.1109/EMCCompo.2013.6735202>.
- [29] A. Boyer, A. Cisse, S. Ben Dhia, L. Guillot, B. Vrignon, Characterization of the evolution of integrated circuit emissions after accelerated aging, *IEEE Trans. Electromagn. Compat.* 51 (4) (2009) <http://dx.doi.org/10.1109/TEMC.2009.2033577>.
- [30] A. Boyer, S.B. Dhia, Effect of aging on power integrity of digital integrated circuits, in: 2013 14th Latin American Test Workshop-LATW, 2013, pp. 1–5, <http://dx.doi.org/10.1109/LATW.2013.6562681>.
- [31] G. Yang, *Accelerated Life Tests*, in *Life Cycle Reliability Engineering*, John Wiley & Sons, Inc, 2007, pp. 252–265.
- [32] J.F. Lawless, *Statistical Models and Methods for Lifetime Data*, second ed., Wiley & Sons, Inc, 2002, <http://dx.doi.org/10.1002/9781118033005>.