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Degradation and Reliability Modeling of EM Robustness of Voltage Regulators Based on ADT: An Approach and A Case Study

Jaber Al Rashid, *Student Member, IEEE*, Mohsen Koohestani, *Senior Member, IEEE*, Laurent Saintis, and Mihaela Barreau

Abstract—This paper presents an approach to develop degradation and reliability models of analog integrated circuit (IC) voltage regulators based on the long-term evolution of the electromagnetic compatibility (EMC) performance degradation due to the stress time-dependent accelerated degradation test (ADT). The ADT plan is designed and conducted on six samples of both UA78L05 and L78L05 ICs placed inside a climatic chamber combining both the thermal step-stress (i.e., 70-110 °C) and constant electrical overstress (i.e., 9 and 12 V) conditions for a total stress duration of 950 hours. All the selected UA78L05 and L78L05 samples are subjected to the direct power injection (DPI) measurement test under nominal conditions in order to characterize their immunity to electromagnetic interference (EMI). The statistical degradation data (i.e., the average injected power) of the aged samples is computed across the entire DPI frequency range for a variety of stress time duration. The proposed log-linear accelerated life-stress test (ALT) model is combined with the Weibull unreliability distribution function model to estimate the failure lifetime data against the applied voltage stress at three different failure threshold criterion. At various constant voltage overstress and threshold constraints, the lifetime reliability performance parameters (i.e., time-to-failure, probability of failure, model constants) of the tested device under tests (DUTs) were evaluated based on the measured degradation data. It is demonstrated that, for a limited number of samples under the combined influence of thermal step-stress with voltage overstress conditions, the proposed reliability model predicts with a very acceptable accuracy the lifetime reliability of both UA78L05 and L78L05 tested ICs, developed based on the conducted immunity degradation data. The physics-based modeling approach is utilized to develop the model for the degradation paths based on the observed monotonic degradation of the measured degradation data as well as the conditions of the thermal step-stress ADT. In order to estimate the unknown parameters of the developed degradation model, the maximum likelihood estimation (MLE) method is combined with a genetic optimisation algorithm.

Index Terms—step-stress ADT, DPI, ALT, physics based model, Weibull distribution, time-to-failure, reliability function

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I. INTRODUCTION

Analog ICs in electronic systems demonstrate significant evolution of their EMC performance when subjected to external environmental (i.e., temperature, humidity, electrical overstress) conditions. Considering the accelerated aging of IC-level electric circuits, reliability analysis is essential for estimating the lifetime of a device. During the operational lifetime of the ICs in nominal environmental conditions, these electronic components experience various internal failure mechanisms in extreme environments (i.e., gate oxide defect, electromigration, hot carrier injection, bias transistor instability, and mobile ion contamination) due to high or low temperature, humidity, and positive or negative biasing electrical overstress, resulting in the formation of cracks, holes and trapping of charge carriers in the gate oxide layer [1], [2]. Consequently, the aging of an IC's internal metal-oxide semiconductor transistors (i.e., threshold voltage, drain-saturation current, and electron mobility) may alter its operational characteristics (noise, leakage current, propagation delay, operating frequency, and gate oxide capacitance) [3]. During the accelerated aging process, degradation or intrinsic failure mechanisms are activated, resulting in a significant impact on the EMC conducted immunity and emission performance of the ICs operating within the electronic system [4]. Multiple stress factors accelerate the aging process, allowing the acceleration rate of the relevant wear-out processes to rise depending on the size and duration of the stresses [5], [6].

Different types of ALTs can be performed to extract reduced lifetime failure data after the component fails permanently due to the application of external stress factors of varying magnitude for a fixed duration [7]. ADTs can be conducted to compute pseudo lifetime failure data based on a predefined degradation criterion without enduring permanent or hard failure. The goal of these elevated stress tests is to determine the DUT's lifetime reliability, failure rate, and other functional parameters or characteristics under normal operating conditions [8]. The acceleration factor (AF) associated with a degradation mechanism induced by a known ageing stress condition can be computed using reduced lifetime failure data obtained during the short duration of the test, and the extracted data of the DUT can be extrapolated for any defined environmental condition [3]. Acceleration law models (i.e., Arrhenius, Eyring) are required for extrapolating the computed failure time data obtained from the accelerated ageing tests so

that the long-term lifetime reliability of the tested components can be predicted for any tested or untested conditions [7], [9]. Moreover, these reliability acceleration tests enable the development of various reliability modeling functions for each corresponding ageing stress levels depending on the defined stress conditions [7]. Considering the fact that acceleration law can be computed from the trend of the reliability functions at different stress conditions, the performed accelerated ALTs for the short duration lead to the determination of the tested component reliability quantitatively at the nominal operational condition [10].

ADT is regarded as a suitable method for estimating the lifetime reliability parameters of electronic components. Considering the difficulty to determine the reliability assessment of highly reliable components operating in nominal environmental conditions, the ADT plan should be designed and conducted at high stress levels to accelerate performance degradation metrics (i.e., voltage, current and power), thereby enabling the prediction of lifetime reliability data in nominal or other environmental conditions [11]. Developing accurate degradation path modeling is essential before predicting reliability parameters of electronic components in an electronic system. Various types of degradation modeling approaches (i.e., general degradation path and stochastic process) were employed in prior research studies to examine the random ADT data [12]- [16]. In [12], a stochastic process was used to develop the best fitting degradation path model using ADT measurement data for DC film capacitors under the influence of the specified humidity stress conditions. Inverse Gaussian [13] and the Wiener process [14] modeling approach were considered to develop the degradation model, taking into account of the measured functional performance degradation data of the tested components (i.e., lithium ion batteries, light-emitting diodes and so on).

Due to the rising demand for dependable and long-lasting products, degradation and reliability modeling analysis have emerged as essential elements in the design and development of electronic systems. Previous research studies have demonstrated different approaches involved for analyzing those proposed degradation and reliability models. In [17]- [18], the MLE method was employed to estimate the unknown constants of the developed degradation models. In [19], degradation model was proposed with standard deviation function and random regression coefficients based on the observed linear deviation of the semiconductor's threshold voltage over time. In [20], predictive failure time distribution using the Monte Carlo simulation, prior to evaluating the reliability of the tested component. Moreover, the reliability modeling approach was demonstrated to predict the reliability of the digital circuit (i.e., SRAM) as a function of time using the developed reliability tool [21], and by applying an extended building-in reliability method [22], while taking into account of the wafer-level reliability system. In [23], the effect of high-temperature stress on the wire bonds were investigated by studying the commonly used physics-of-failure lifetime reliability models for wire bond interconnects, available in power electronic modules. In [24], both the developed electrical simulation and degradation models for the analog voltage regulator circuit

were considered in order to predict pseudo failure time and the related developed reliability model parameters, when subjected to the defined constant multiple stress (i.e., high thermal and electrical overstress) conditions.

Numerous research studies were conducted to compare the EMC performance before and after the ageing process performed on both analog and digital ICs. In accordance to the AEC-Q-100-Rev F standards [25], the accelerated ageing tests were conducted to investigate the ageing impact on the evolution of the electromagnetic robustness of various ICs (i.e., phase-locked loop, microcontroller, operational amplifier), which was compared to the conducted immunity and emission models [26]- [28]. In [26], a simulation model was constructed to predict the long-term conducted immunity of various internal circuit blocks of an aged phase-locked loop, which was compared to the DPI measurement data obtained in accordance with the IEC 62132-4 standard [29]. To predict the EMC evolution of the investigated analog circuits, the effect of ageing induced by external environmental (temperature and electrical voltage) stress factors was incorporated into the developed conducted immunity model [30]. The influence of ageing is integrated on the developed integrated circuit immunity model-conducted immunity (ICIM-CI) of the tested voltage regulator ICs were investigated [31]. In [32], the impact of aging on the EMC performance of a Spartan6 Xilinx field-programmable gate array (FPGA) digital circuit device was studied to predict the long-term conducted emission level by proposing a new methodology, which involved constructing the conducted emission model for the tested FPGA, while accounting for accelerated ageing using the predictive multi-stressors reliability model (M-STORM).

Prior research studies investigated on predicting the lifetime reliability based on the conducted emission of the digital ICs. However, to the best of our knowledge, the development of both degradation and reliability models based on the conducted immunity performance degradation of ICs have not yet been investigated. The use of combined thermal and electrical overstress conditions to characterize the conducted immunity of analog and digital ICs for accurately estimating their degradation and reliability model parameters have not yet been studied. Thus, the current study aims to demonstrate the ALT and ADT modeling approach by combining for determining the the life-stress acceleration laws combined with various statistical distributions (i.e. Weibull, Lognormal) to determine the lifetime reliability and predict the EMC performance degradation of analog voltage regulator ICs under the combined influence of both the constant electrical overstress and thermal step-stress conditions. The paper is categorized into following sections. Section II highlights the experimental methodology involved for characterizing the conducted immunity degradation under the specified ADT plan. Section III demonstrates the conducted immunity measurement results of the tested ICs, followed by presenting ALT and ADT modeling approach in section IV and V respectively.

II. MATERIALS AND METHODS

This section deals with the design of the ADT plan as well as the measurement setup used to perform the accelerated

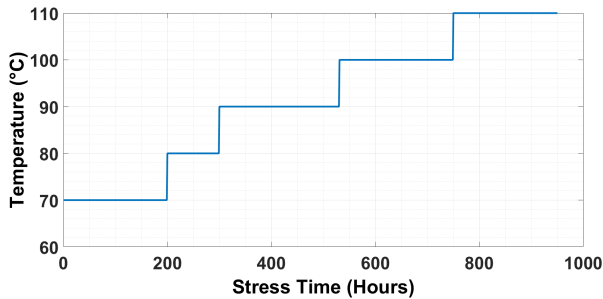


Fig. 1. The step-stress ADT plan.

TABLE I

AGING STRESS CONDITIONS TO PERFORM THE ADTs ON THE ICs

IC reference	Samples	Electrical voltage stress	Temperature stress	Total stress duration
L78L05	S1, S2 and S3	9 V	70 – 110 °C	950 hours
	S4, S5 and S6	12 V	70 – 110 °C	950 hours
UA78L05	T1, T2 and T3	9 V	70 – 110 °C	950 hours
	T4, T5 and T6	12 V	70 – 110 °C	950 hours

aging test on the selected functionally identical and pin-to-pin compatible voltage regulator ICs developed by two different manufacturers (i.e., STMicroelectronics L78L05 and Texas Instruments UA78L05). The test samples were mounted on a generic SOIC8 extraction test board made of a 4-layer FR4 PCB (Fig. 2b).

A. The ADT Plan

The step-stress ADT plan was designed to accelerate the aging process of the ICs depending on the choice of multiple stress types (i.e., thermal and electrical voltage), magnitude and total duration. Fig. 1 depicts the considered high temperature step-stress ADT, whereas Table I provides information on the number of IC samples under the influence of both temperature and electrical overstress conditions. The magnitude of the temperature stress is incremented between 70 and 110 °C with a linear step-size of 10 °C for a total stress time duration of 950 hours. Fig. 1 shows that both the lowest and highest temperature stress is kept constant applied for 200 hours. However, from 80 °C to 110 °C, the thermal was observed at different stress time (i.e., 300, 531 and 645 hours, respectively). A total of twelve test samples (i.e., T1-T6 and S1-S6) were considered to obtain an accurate enough estimation of the EMC performance degradation caused by the accelerated aging process. Hence, sufficient number of IC components (i.e., 6 units) for both L78L05 and UA78L05 were selected instead of a single sample for observing EMC level dispersion between the tested samples, which could provide a clear reflection on the EMR characteristics of the DUTs that belongs to the entire family of the L78L05 and UA78L05.

Table I shows a similar thermal stress magnitude and duration with two different constant electrical overstresses voltage levels (i.e., 9 V and 12 V) applied on the IC samples. Among the six L7805 samples, S1, S2 and S3 were selected for aging at 9 V, and the rest of the three IC samples (i.e.,

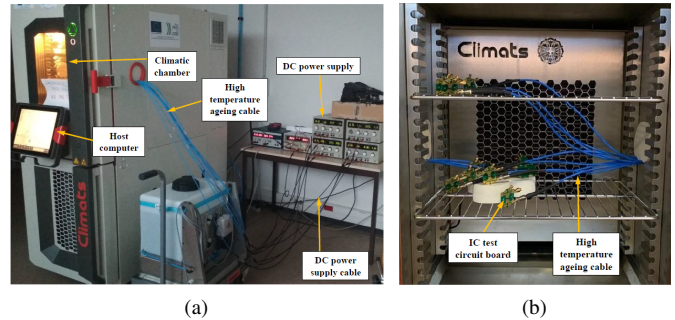


Fig. 2. Experimental test setup: (a) outside and (b) inside views of the climatic chamber.

S4, S5 and S6) were subjected to aging at constant 12 V electrical overstress condition. Similarly, three samples (i.e., T1, T2 and T3) of UA78L05 were subjected to low electrical overstress, while the rest of the UA78L05 samples (i.e., T4, T5 and T6) were allowed to undergo through the accelerated aging process under high electrical overstress condition during the ADT performed inside the thermal climatic chamber. It should be stated that since for input voltages within the range of 15 to 20 V all the IC samples were crashed after 200 hours of aging under the first thermal stress magnitude (i.e., 70 °C), V_{in} stress of 20% and 60% higher than the selected 7.5 V applied voltage in nominal operating condition was considered in the ADT plan.

B. Measurement Setup and Procedure

The experimental setup to perform the ADT on the selected IC samples is displayed in Fig. 2. The high temperature stress was applied on the DUTs inside the climatic chamber. The host computer was used to program the temperature-controlled Spiral V software integrated with the climatic chamber (Fig. 2a) to implement the designed ADT plan. Multi-channel DC voltage power supplies were utilized to provide constant electrical voltage stress into the DC input voltage (V_{in}) pin of the tested ICs. Thermal resistant aging cables [33] were connected to the tested samples inside the climatic chamber to inject both low and high electrical overstress voltage levels into the V_{in} pin 8 of the tested DUTs (Fig. 2b).

C. Experimental Methodology

The aging stress time-dependent ADTs was conducted on the DUTs inside the climatic chamber to ensure permanent degradation induced by the applied stress conditions. During the accelerated aging process, after a certain stress duration according to the methodology shown in Fig. 3, the process was paused and DUT tests were performed on all the fresh and aged DUTs to evaluate the conducted immunity variations. The process was then resumed until the completion of the ADT plan.

Stress-measurement-stress refers to the repetitive cycle of applying both thermal and electrical aging stress on the IC samples inside the climatic chamber during the ADT for a fixed aging stress-time (T'), followed by removing the stress

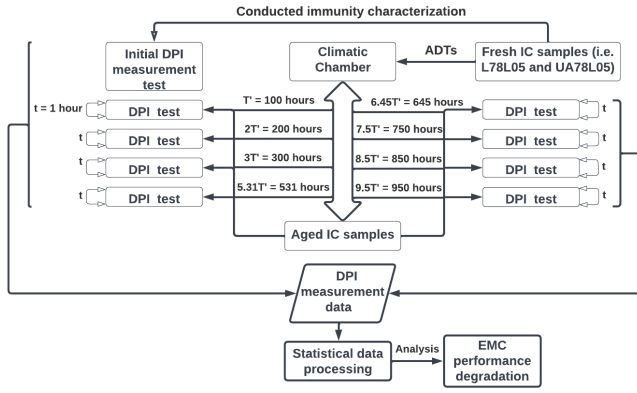


Fig. 3. Time-dependent accelerated aging methodology.

and performing the DPI test on these aged samples outside the climatic chamber under the nominal conditions (i.e., 25 °C and 7.5 V) for a very short time (t) period. Note that, little time duration of t was maintained compared to that of the T' in order to ensure that the aged ICs would not undergo into partial recovery from the permanent degradation induced by the ADTs. It was observed that all of the tested DUTs of UA78L05 and L78L05 remained operational and did not exhibit permanent failures after the ADTs were completed.

D. DPI Test Procedure and Measurement Algorithm

The DPI measurement setup is similar to that presented in [34] is implemented with the measurement algorithm shown in Fig. 4b. Fig. 4a shows the standard DPI test bench setup consisting of the DPI equipments for characterizing the conducted immunity of the DUT. The standard DPI experimental methodology was performed in accordance to the IEC 62132-4 standard [27]. The LabVIEW software, which is integrated with the DPI test bench, has been programmed based on the DPI algorithm to measure and record the relevant DPI power injected (i.e., P_{inj}) data at different corresponding DPI frequencies. The flowchart of the DPI measurement algorithm is displayed in Fig. 4b. The step-by-step procedures required to implement this algorithm is mentioned as follows.

- 1) choose the minimum and the maximum generated power of the RF signal, which is denoted by P_{min} and P_{max} , respectively.
- 2) select both the initial and final frequency of the amplified RF signal, ranging between 10 and 1000 MHz.
- 3) define the DPI failure criterion (i.e., $\pm 4\%$) deviation from the nominal output voltage (V_{out}) on all the DUTs.
- 4) considering a fixed DPI frequency, vary the generated power of the RF signal between -40 dBm and $+13$ dBm with a linear increment of 1 dBm.
- 5) check if the defined failure threshold criterion is reached for any specific generated power and the DPI frequency value.
- 6) when the DPI failure occurs due to the DC offset (i.e., ± 0.2 V) variation at the V_{out} pin 1 of the tested samples occurs, measure and record the forward power, reflected power using the power meters, and the minimum P_{inj}

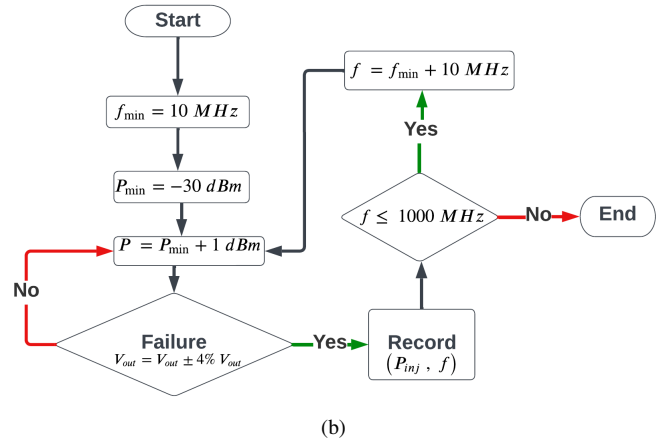
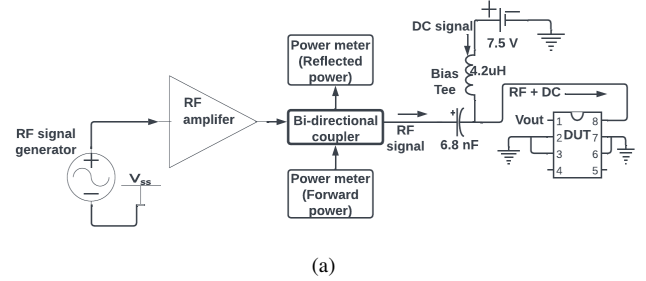


Fig. 4. (a) DPI test bench setup, (b) flowchart of the DPI measurement algorithm.

coupled to the V_{in} pin 8 of the DUT at the corresponding frequency.

- 7) vary the DPI frequency (f) between the initial and final value with a linear step-size of 10 MHz. Repeat the above measurement steps to record the computed P_{inj} at each corresponding frequency values.

III. EXPERIMENTAL RESULTS AND ANALYSIS

This section presents the DPI measurement results performed on the tested DUTs before and after the accelerated aging at different stress duration. The evolution of the conducted immunity drift under the influence of aging induced by the defined stress conditions applied on the 6 samples of L78L05 and UA78L05 at various stress duration has been discussed.

A. Conducted Immunity Drift of the Aged ICs

The DPI measurement tests were performed on all the selected fresh and aged DUT samples of UA78L05 and L78L05 to measure the P_{inj} data at each corresponding DPI frequency value. Power injected drift (ΔP_{inj}) caused by accelerated aging was calculated for each DPI frequency value ranging from 10 to 1000 MHz to investigate the impact of aging on the deviation of the conducted immunity level at different aging stress times. The corresponding ΔP_{inj} data was extracted at each tested frequency by subtracting the measured P_{inj} of the fresh sample from that of the aged state. Both Figs. 5 and 6 depicts the computed ΔP_{inj} data in the DPI frequency domain at different ageing stress time intervals. A negative (positive) drift implies reduction (improvement) in

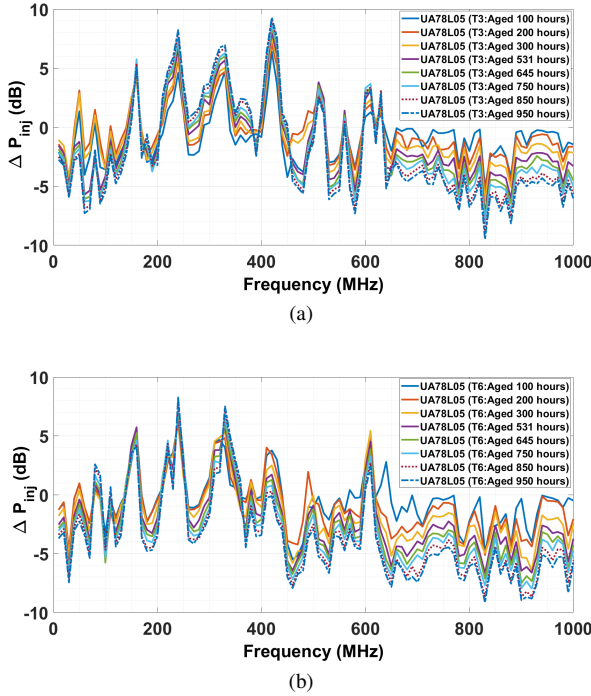


Fig. 5. Conducted immunity level drift of UA78L05 samples at various stress duration caused by the thermal step-stress as well as (a) low and (b) high voltage overstress.

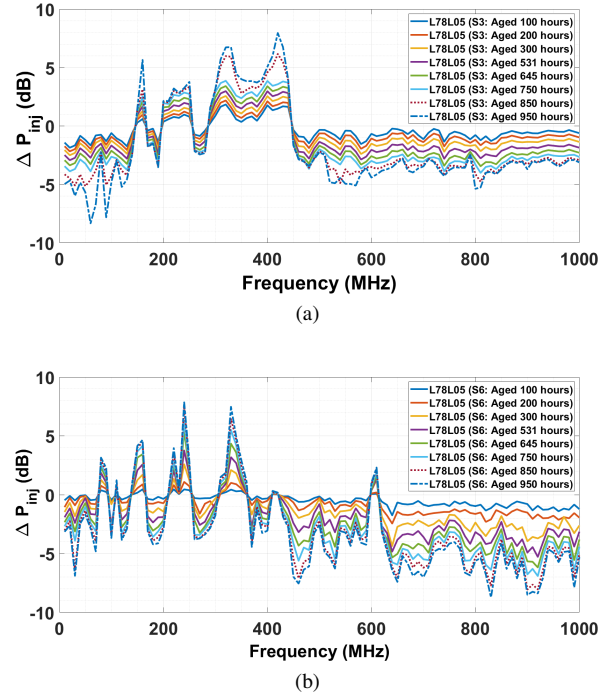


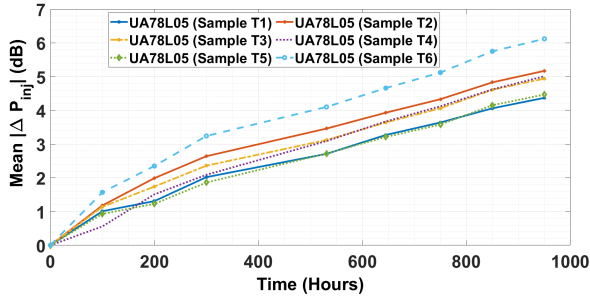
Fig. 6. Conducted immunity level drift of L78L05 samples at various stress duration caused by the thermal step-stress as well as (a) low and (b) high electrical overstress.

the conducted immunity level of the aged samples. Fig. 5a illustrates that the absolute mean ΔP_{inj} of the aged T3 sample increased between 1.7 and 4.3 dB over the whole frequency range, while the absolute average ΔP_{inj} for the T6 reached from 1.8 dB to 4.7 dB between 100 and 950 hours of aging applied at the constant high electrical overstress as shown in the Fig. 5b. Fig. 6a demonstrates a lower mean immunity level drift at every stress duration, reaching an absolute value of 3.9 dB at the end of the thermal step-stress ADT compared to the 4.4 dB extracted over the entire frequency range of interest as shown in Fig. 6b. It should be noted that all the remaining UA78L05 and L78L05 IC samples showed a similar evolution on the conducted ΔP_{inj} data across the entire tested frequency domain, depending on the applied magnitude and duration of the stress; results are not provided for the sake of brevity. This observed dispersion in the EMC performance level among the DUTs of the tested ICs can be due to the process variations between these tested samples, which leads to the numerical variations of the internal transistor parameters (i.e., saturation current, length and width, current gain) of the identical CMOS transistors with similar functionality but different references used in the design phase.

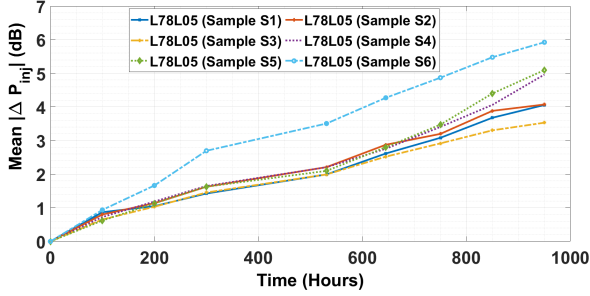
Moreover, the origin of the observed EMC degradation behavior can be either due to the modification of the internal NMOS and PMOS transistor's electrical parameters (i.e., V_{th} and the μ_{eff}), different manufacturing date, or different physical failure mechanisms (i.e., gate oxide defect, electromigration, and mobile ion contamination) leading to cracks and holes in their internal structure (e.g. gate oxide and metal layers) [35] [36]. Hence, these prevalent intrinsic failures of CMOS circuit transistors within the tested ICs are

responsible for the internal parametric drift, resulting in a significant EMC level drift caused by aging. The influence of higher number of samples was confirmed to have no impact on the EMC dispersion between the tested samples. An increase in the number of DUTs, on the other hand, would allow for more measurement data on EMC degradation and lifetime failures, which might improve the accuracy of predicting the proposed reliability model's unknown parameters and widen its confidence interval to predict the failure probability distribution of the developed model.

Fig. 7 depicts the EMC performance degradation curves of all the tested samples as a function of the aging stress time. Since the ΔP_{inj} of the aged DUTs was dependent on both frequency and stress time, mean absolute injected power drift ($|\Delta P_{inj}|$), computed at various stress time by taking the average of the absolute ΔP_{inj} data for every corresponding frequency, was considered the suitable EMC performance degradation indicator parameter. At each stress duration, the corresponding EMC degradation data was characterized by evaluating the magnitude of the mean $|\Delta P_{inj}|$ over the high frequency range (i.e., 600-1000 MHz). The latter band was chosen due to the continuous monotonic immunity degradation (Fig. 5), which leads to model the EMC degradation behavior of the DUTs with higher accuracy. Figs. 7a and 7b show significant increment of the mean $|\Delta P_{inj}|$ (with a higher positive slope in UA78L05 compared to L78L05 samples) with increasing stress duration under the defined ADT plan. The immunity degradation of both UA78L05 and L78L05 could be compared by highlighting the noticeable difference in the mean $|\Delta P_{inj}|$ depending on the applied stress time. The aged T6 showed highest variation in the mean $|\Delta P_{inj}|$



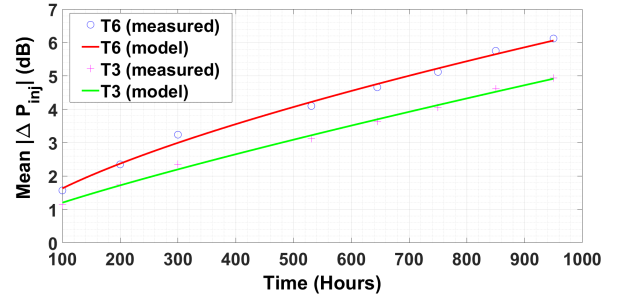
(a)



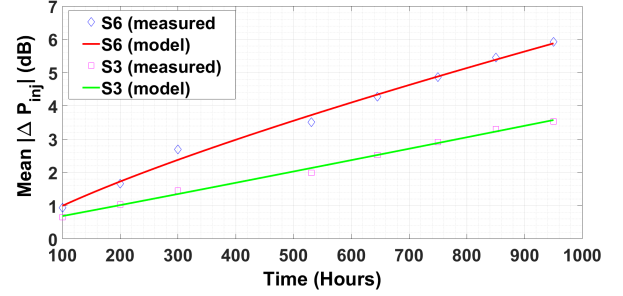
(b)

Fig. 7. Conducted immunity degradation as a function of the stress time on the tested samples of (a) UA78L05, (b) L78L05.

compared to the other tested samples in every time intervals, reaching a maximum value of 6.12 dB at 950 hours (Fig. 7a). However, lower mean $|\Delta P_{inj}|$ values over the high desired frequency range could be observed for the L78L05 sample ICs (Fig. 7b). After the completion of 950 hours, the aged L78L05 samples S3 and S6 demonstrated a 28.5% and 3.26% lower immunity degradation compared to those of the aged UA78L05 T3 and T6. Fig. 8 showcases the good agreement between the generated degradation paths fitted to the measured EMC degradation data by linear regression technique as shown in Fig. 7 for two samples of UA78L05 and L78L05 at different stress duration. The mathematical expression which represents these EMC degradation curves is similar to that of the equation (11). The similar monotonic degradation increasing with stress duration trend implies that the same degradation model can be employed for both UA78L05 and L78L05 ICs to estimate the unknown relevant parameters of the model predicting the conducted immunity degradation. Applying the linear regression analysis to generate the best-fit degradation path curves (Fig. 8) allowed for the determination of the mathematical relationship between the absolute mean ΔP_{inj} and stress time (t), with a time exponent stress-dependent (γ) variable used in (11). The typical numerical value for the γ parameter was found to be 0.64 and 0.51 for T3 and T6, respectively (Fig. 8a). On the other hand, the γ parameter for L78L05 (i.e., S3 and S6) degradation curves (Fig 8b) were 0.75 and 0.80, respectively. Hence, these above aforementioned numerical values could be considered to be comparable to that of stated in [37]. It is worth mentioning that the typical value of the defined time exponent γ parameter varies depending on the specified stress conditions.



(a)



(b)

Fig. 8. Degradation path fitted to the EMC degradation data of ICs samples (a) UA78L05, (b) L78L05.

IV. ACCELERATED LIFE TEST MODELING: RELIABILITY ANALYSIS OF THE DUTS

This section presents the ALT modeling methodology based on the EMC performance degradation data obtained on the tested DUTs. This developed ALT model is used to estimate unknown ALT model parameters and predict the lifetime reliability of the aged IC regulators under the influence of different constant electrical overstress conditions and failure threshold (G) criterion considered on the conducted immunity degradation of the tested IC samples.

A. ALT Reliability Modeling and Parameter Estimation

Inverse-power voltage (IPV) law and the temperature dependent Eyring ALT models were used to develop a quantifiable life-stress model to predict the lifetime stress data [9]. The Eyring model is the modified Arrhenius ALT model, which can be mathematically expressed as a function of the temperature or humidity stress only, as can be seen in (1), where $L(T)$ refers to the lifetime data that can be computed as a function of single stress T , A_x and B_x are the stress-dependent unknown model constants. The IPV acceleration law model due the voltage stress only can be expressed in (2), where $L(V)$ represents the lifetime of a component as a function of voltage stress only that increases the acceleration factor and performance degradation of the DUT, C and n refers to the model parameters that can be determined analytically by using different distribution function (i.e., exponential, log-normal and Weibull). Weibull distribution on the degradation is considered to be suitable for obtaining information on the failure modes or mechanisms and characterize both the useful life and wear-out phase in the bathtub curve of the tested

samples [24]. Equation (3), natural logarithmic form in (3), is the combination of equations (1) and (2) to develop a mathematical model for the lifetime multiple stress parameters dependent acceleration model. The analytical expression in (3) also contains unknown model constants (C_x , n and B_x), which can be estimated with high precision depending on the accuracy of the model.

$$L(T) = \frac{1}{T} e^{-(A_x - \frac{B_x}{T})} \quad (1)$$

$$L(V) = \frac{1}{C_x V^n} \quad (2)$$

Equation (4) is considered the location parameter (μ_x), which refers to the mean time-to-failure (TTF) of the tested sample. Thus, equation (4) was modified, and the proposed lifetime acceleration model was developed as expressed in (5), where $\mu_x(V, T, G)$ is a function of three independent variables, i.e. voltage V and temperature T stresses while considering G as the failure threshold constraint, and α_{x_0} , α_{x_1} , α_{x_2} and α_{x_3} are the stress-dependent model constants. According to Fig. 8, the influence of V stress can be seen to be more significant compared to T , hence, equation (5) can be further simplified to (6) for a fixed G criterion.

$$L(T, V) = \frac{A_x}{V^n} e^{\frac{B_x}{T}} \quad (3)$$

$$\mu_x(V, T, G) = \ln L(T, V) = \ln A_x - n \ln V + \frac{B_x}{T} \quad (4)$$

$$\begin{aligned} \mu_x(V, T, G) &= \ln L(T, V, G) \\ &= \alpha_{x_0} + \alpha_{x_1} \ln(V) + \alpha_{x_2} G + \alpha_{x_3} \frac{1}{T} \end{aligned} \quad (5)$$

$$\mu_x(V, G) = \alpha_{x_0} + \alpha_{x_1} \ln(V) + \alpha_{x_2} G \quad (6)$$

In order to construct the reliability model of the DUTs, the combination of applying the Weibull's distribution on the proposed lifetime ALT model expressed in (6) for extracting the relevant ALT model constants and estimating reliability parameters with good accuracy for the defined accelerated tested conditions were considered. The expressions for the CDF, PDF, and natural logarithmic form of the PDF of the Weibull distribution are respectively given in (7), (8) and (9), where η and β_w refer to the scale and shape parameters, respectively. The overall combination of the proposed ALT-Weibull reliability model can be then expressed by substituting the ALT proposed model for the applied V and G mentioned in (6) into the term $\ln \eta$ in (9). Hence, the simplified analytical expression for the developed ALT-Weibull reliability model is given in (10), with unknown model parameters of α_{x_0} , α_{x_1} , α_{x_2} , β_w and η .

$$F_w(t) = 1 - e^{-(t/\eta)^{\beta_w}} \quad (7)$$

TABLE II
ALT RELIABILITY MODEL PARAMETERS FOR BOTH L78L05 AND UA78L05

Model parameters	IC reference	
	UA78L05	L78L05
α_{x_0}	3.46	6.04
α_{x_1}	0.16	0.14
α_{x_2}	0.41	-0.57
β_w	4.60	6.83
η	694.85	1074.17
L_f	-105.69	-102.30

$$f_w(t) = \frac{\beta_w}{\eta} \cdot \left(\frac{t}{\eta}\right)^{\beta_w-1} \cdot e^{-\left(\frac{t}{\eta}\right)^{\beta_w}} \quad (8)$$

$$\ln f_w(t) = \ln \beta_w - \ln \eta + (\beta_w - 1)(\ln t - \ln \eta) - \left(\frac{t}{\eta}\right)^{\beta_w} \quad (9)$$

$$\begin{aligned} \ln f_w(t) &= \ln \beta_w - (\alpha_{x_0} + \alpha_{x_1} \ln(V) + \alpha_{x_2} G) + (\beta_w - 1) \\ &\quad \times [\ln t - \mu(V, G)] - \left(\frac{t}{\eta}\right)^{\beta_w} \end{aligned} \quad (10)$$

Those unknown reliability model parameters were obtained for both DUTs by applying the MLE method on the developed ALT-Weibull model (10). With the help of the Weibull distribution, which is applied on the pseudo TTF data obtained from the degradation data measurements under the specified G and V conditions, the MLE method allows to estimate these reliability model parameters. Table II provides the estimated values for the proposed reliability model parameters under the nominal conditions of 7.5 V and 15% criteria on the evaluated EMC degradation data for the tested samples of both L78L05 and UA78L05. The almost close L_f values for both L78L05 and UA78L05 regulators implies that the model fits to the data measurements of the tested ICs. Moreover, significant difference in the scale parameter η of the Weibull distribution might be due to the different model constants obtained by Weibull++ software under the defined accelerated life test conditions. The positive and greater than one β_w value indicates that both L78L05 and UA78L05 DUTs were degraded in the bathtub curve's wear-out phase with increasing failure rate.

B. Reliability and Life-data Analysis of DUTs

The lifetime reliability of the tested samples is characterized under the impact of applying two different constant electrical voltage stresses (i.e., 9 V and 12 V) on both UA78L05 and L78L05 based on the EMC degradation observed during the ADTs. Fig. 9 demonstrates the Weibull distribution plots of the unreliability function, which fits to the pseudo TTF degradation data of UA78L05 and L78L05 IC DUTs for two different stress conditions at three different G criterion (i.e., 5%, 10% and 15%). Time on the x -axis refers to the computed pseudo TTF based on the EMC degradation data under the specified threshold criterion, whereas the data points in the

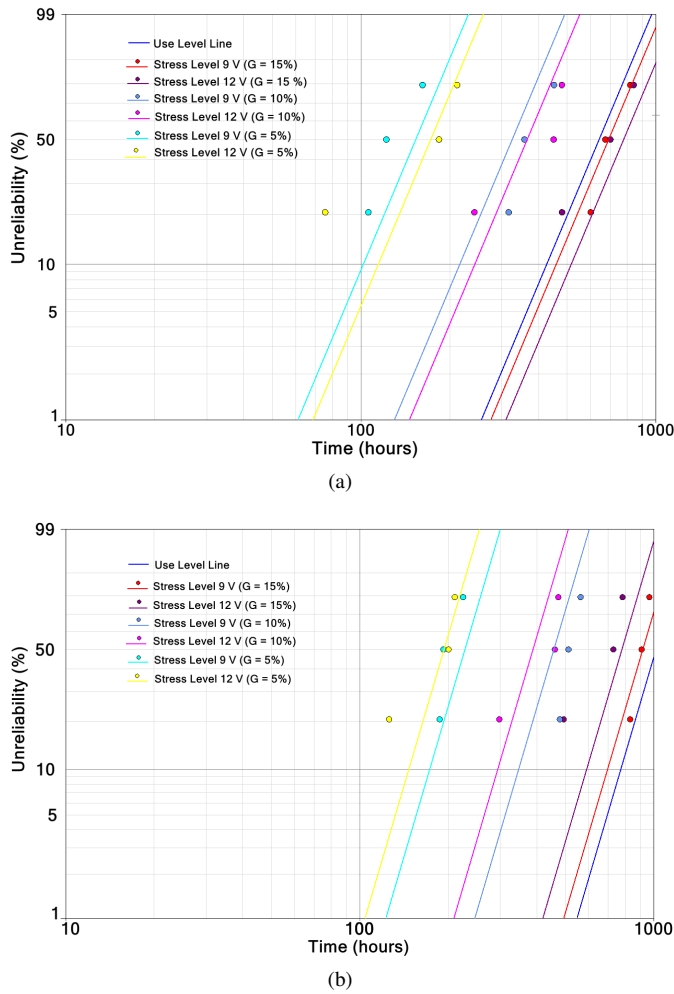


Fig. 9. lifetime reliability Weibull distribution fits to pseudo failure time at different stress conditions applied on (a) UA78L05, (b) L78L05.

y -axis corresponds to the predicted unreliability (probability of failure). When the observed EMC degradation path reaches the defined G criterion (i.e., 15%) in the nominal condition (Fig. 8), the corresponding pseudo TTF of the tested DUTs could be determined by considering the G as the ratio of mean $|P_{inj}|$ to that of mean P_{inj} at different DPI measurement time. The logarithmic fits to these data points is represented by the parallel lines, which are produced due to applying the Weibull distribution on the proposed lifetime reliability model. Note that the limited number of tested IC samples could be responsible for observing the mismatch between these parallel lines and the pseudo TTF data points as shown in Figs. 9a and 9b. The best fit parallel lines were plotted in Fig. 9 for different stress levels, considering the β_w parameter is fixed irrespective of the stress magnitude unlike the η parameter, but depends on the stress types applied on the tested IC samples. This limitation might be resolved by increasing the number of tested IC samples, which would minimize the observed discrepancy between a large number of TTF data points and logarithmic best-fit parallel lines, and the developed ALT model's precision could be enhanced.

Fig. 9a demonstrates the unreliability with corresponding pseudo TTF when all six samples were subjected to the defined

G for both 9 V and 12 V stress levels above the use level, which refers to the nominal conditions (i.e., 7.5 V and 25°C at 15% criterion). It can be observed that the unreliability of all tested samples varies from 20% to 80%, with a larger pseudo TTF for the 10% criterion (485 hours at 12 V with 80% unreliability) compared to the 5% (220 hours at 12 V with 80% unreliability). For a fixed G criterion, an inverse relationship between the considered voltage stress and pseudo TTF was noticed for samples of L78L05 compared to UA78L05 (Fig. 9), which is due to the noticeable difference in the conducted immunity degradation of the tested DUTs.

Fig. 9b shows that at a fixed G criterion, the pseudo TTF of the majority of L78L05 samples is found to be greater at 12 V than at 9 V applied stress. Applying the proposed lifetime reliability model to the tested samples of L78L05, the greatest unreliability is observed at approximately 478 hours when a 10% failure criterion is applied to the EMC performance degradation of a single aged unit under 12 V overstress conditions. On the other hand, when applying the same stress level and G criterion, the sample is considered unreliable after 300 hours with the least unreliability. Moreover, under the influence of 12 V and 10% criterion with 50% unreliability, higher pseudo TTF (around 518 hours) was computed for one of the L78L05 sample compared to that of the UA78L05 sample, whose TTF was 454 hours with the identical predicted unreliability at the same applied V and G constraints.

Fig. 10 shows the reliability (or survival probability) line best fits to the EMC degradation data of the tested samples under the influence of the defined failure G criterion and voltage stress conditions. The reliability values on the y -axis corresponds to the non-failure probability for each data points against the pseudo TTF on the x -axis. Considering three different G criteria and applying two different voltage overstress levels, a total of 18 degradation data points were plotted for both UA78L05 and L78L05 samples.

Considering 10% criterion at 12 V applied stress level, the 96% reliability and unreliability model functions for a tested sample occur at 245 and 850 pseudo TTF hours, respectively (Fig. 10a). Thus, all the tested samples of UA78L05 subjected to different constraints would fail within the total applied stress duration. However, as observed in Fig. 10b, unlike the UA78L05, few tested L78L05 samples would fail beyond 1200 hours with a lifetime unreliability of around 84%. Hence, those samples would have the remaining life of only 16% having the survival probability of 0.16 while the constant stress is maintained and a fixed G threshold is defined on the degradation data.

Fig. 10b shows similar behaviour of the proposed reliability model function, which decreases with increasing failure time expressed in hours and this reliability curve best fits to the degradation data points of the DUTs at 9 and 12 V stress magnitude. It is predicted that all the tested aged L78L05 samples would survive upto 100% until 400 hours, and the highest reliability or the lowest probability of failure is observed at 640 hours when the degradation data crosses or reaches the defined failure G level under the impact of applying a constant stress.

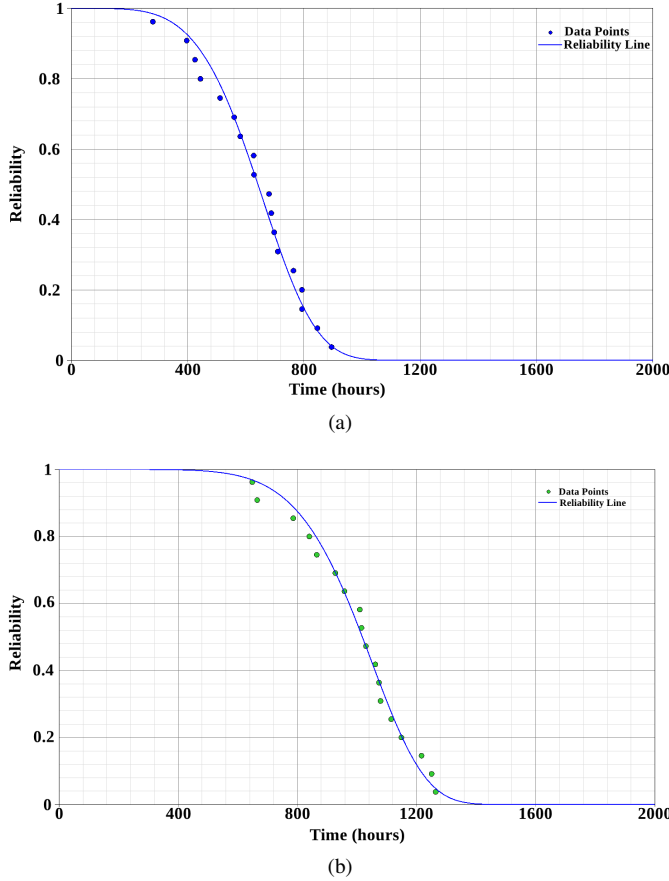


Fig. 10. Reliability function based on the proposed ALT model fits to the degradation data of (a) UA78L05, (b) L78L05.

V. DEGRADATION PATH MODELING OF THE DUTS BASED ON THE STEP-STRESS ADTs

Due to performing the step-stress ADT on a tested unit, the degradation path function at any stress time could be considered to depend only on the current accelerated stress level applied for the specified time intervals and the observed cumulative degradation accumulated due to applying previous stress levels, but independent of the failure mechanisms, which remains consistent at both accelerated and nominal stress condition [16]. A physics-based approach for degradation modeling was used to estimate the unknown parameters of the selected degradation model and to depict the degradation path caused by the evolution of the monotonic degradation observed at different stress duration over the high frequency range (i.e., 600-1000 MHz) as shown in Fig. 8.

The simplified proposed mathematical model representing the monotonic degradation observed in Fig. 8 is expressed in equation (11), where $g_{ikl}(t)$ corresponds to the degradation function of stress magnitude and stress duration (t), A and γ are the stress-dependent unknown coefficients. Note that the similar mathematical expression was also found in [37], which considered the power MOSFET law to explain behaviour of the stress-dependent degradation path. Applying the logarithm in equation (11) provides the expression for the $d_{ikl}(t)$ as the logarithm of the ratio between the variation of the mean $|\Delta P_{inj}|$ and the computed nominal mean P_{inj} across the DPI

frequency range for the fresh unit tested sample (i) before aging, voltage level (k) and temperature stress level (l) as shown in equation (12). Considering the combined aging impact of the multiple stress factors (voltage and temperature), the term A_{ikl} can be expressed using the accelerated aging law model (i.e., Eyring model) as shown in equation 13. Equation (13) can be modified by substituting the expression of A_{ikl} to obtain the expression as shown in (14), which represents degradation path modeling under the combined influence of temperature (T) and voltage (V) stress on the accelerated aging process. Consequently, the proposed physics-based model for the degradation path ($d_{ikl}(t)$) is expressed in (15), with unknown degradation parameters (i.e., β_1 , β_2 , β_3 and β_4). By comparing and equating both equations (14) and (15), these unknown parameters can be determined as shown in (16), where β_1 is found by the normal distribution of μ_α and σ_α , E_a is the activation energy expressed in eV, K is the Boltzmann constant measured in eV/°C. The best fits of this proposed degradation model to the EMC degradation data indicate that the modeling methodology is adequate enough to estimate the unknown variables B , α_i and γ .

$$g_{ikl}(t) = A_{ikl} \times t^\gamma \quad (11)$$

$$d_{ikl}(t) = \ln\left(\frac{\Delta P_{inj}}{P_{inj}}\right) = \ln(A_{ikl}) + \gamma \ln(t) \quad (12)$$

$$\ln(A_{ikl}) = \ln(\alpha_i) - B \ln(V) + \frac{E_a}{KT} \quad (13)$$

$$d_{ikl}(t) = \ln\left(\frac{\Delta P_{inj}}{P_{inj}}\right) = \ln(\alpha_i) - B \ln(V) + \frac{E_a}{KT} + \gamma \ln(t) \quad (14)$$

$$d_{ikl}(t) = \beta_1 + \beta_2 \ln(V) + \beta_3 \frac{1}{T} + \beta_4 \ln(t) \quad (15)$$

$$\beta = \begin{cases} \beta_1 = \ln(\alpha_i), \text{ where } \alpha_i \sim \ln(\mu, \sigma) \Rightarrow \beta_1 \sim \mathcal{N}(\mu_\alpha, \sigma_\alpha) \\ \beta_2 = -B \\ \beta_3 = \frac{E_a}{K} \\ \beta_4 = \gamma \end{cases} \quad (16)$$

Since thermal step-stress ADT was applied to the DUTs, the cumulative degradation path function for a tested sample unit due to thermal step-stress, denoted by $D_{ik}(t)$, can be represented by a series of mathematical expressions as shown in Eq. (17), where the term τ_m ($m=1, 2, \dots, 5$) refers to the pseudo time needed to obtain the step-stress ADT degradation path value due to the specified T stress level, and t_m refers to the time after which the T stress level increases linearly according to the step-stress ADT plan illustrated in Fig. 1. The term τ_m can be derived by the general relationship between each degradation path functions at different time intervals as shown in Eq. (18). The latter can be used to obtain τ_2 to τ_5 at different intervals of time and T .

$$D_{ik}(t) = \begin{cases} d_{ikl_1}(t) & \text{if } 0 < t \leq 200 \\ d_{ikl_2}(\tau_2 + t - t_1) & \text{if } 200 < t \leq 300 \\ d_{ikl_3}(\tau_3 + t - t_2) & \text{if } 300 < t \leq 531 \\ d_{ikl_4}(\tau_4 + t - t_3) & \text{if } 531 < t \leq 750 \\ d_{ikl_5}(\tau_5 + t - t_4) & \text{if } 750 < t \leq 950 \end{cases} \quad (17)$$

$$\tau_m = \begin{cases} t_1 & m = 1 \\ (\tau_{m-1} + t_{m-1} - t_{m-2}) \exp\left(\frac{\beta_3}{\beta_4} \left(\frac{1}{T_{m-1}} - \frac{1}{T_m}\right)\right) & 2 \leq m \leq 5 \end{cases} \quad (18)$$

where,

$$\begin{aligned} \tau_2 &= \tau_1 \exp\left(\frac{\beta_3}{\beta_4} \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) & \text{if } t_1 < t \leq t_2 \\ \tau_3 &= (\tau_2 + t_2 - t_1) \exp\left(\frac{\beta_3}{\beta_4} \left(\frac{1}{T_2} - \frac{1}{T_3}\right)\right) & \text{if } t_2 < t \leq t_3 \\ \tau_4 &= (\tau_3 + t_3 - t_2) \exp\left(\frac{\beta_3}{\beta_4} \left(\frac{1}{T_3} - \frac{1}{T_4}\right)\right) & \text{if } t_3 < t \leq t_4 \\ \tau_5 &= (\tau_4 + t_4 - t_3) \exp\left(\frac{\beta_3}{\beta_4} \left(\frac{1}{T_4} - \frac{1}{T_5}\right)\right) & \text{if } t_4 < t \leq t_5 \end{aligned}$$

$$\begin{aligned} F_{ik}(t) &= P(d_{ikl}(t) \geq G) \\ &= \Phi\left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T} - \beta_4 \ln(t) - \mu_\alpha}{\sigma_\alpha}\right) \end{aligned} \quad (19)$$

In order to obtain the unknown parameters of the proposed degradation model, the analytic expression for the cumulative distribution function (CDF) was derived for one value of the applied thermal and electrical stress level as shown in (19), where the CDF is denoted by F_{ik} , and ϕ refers to the standard normal distribution of the CDF. This expression was determined based on the condition that the tested sample fail if the proposed $g_{ikl}(t)$, which is a function of t and T , reaches or exceeds the user-defined threshold G criterion based on the functionality outlined in the specifications, and the applications. The latter was considered the ratio of the mean $|\Delta P_{in,j}|$ to that of the nominal mean $P_{in,j}$ of the fresh sample before the step-stress ADT. The performed immunity performance degradation data for all of the tested DUTs at various measurement time durations were taken into account (Fig. 7). Consequently, for the purposes of this ADT modeling, G was calculated for each of the tested DUTs at different durations of stress time, taking the EMC degradation data into consideration. When the observed EMC performance degradation $d_{ikl}(t)$ reached the critical horizontal degradation level (D_v) at the defined G , the pseudo TTF data was also determined for the ALT modeling.

$$F_{ik}(t) = \begin{cases} \Phi\left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_1} - \beta_4 \ln(t) - \mu_\alpha}{\sigma_\alpha}\right) \\ \Phi\left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_2} - \beta_4 \ln(\tau_2 + t - 200) - \mu_\alpha}{\sigma_\alpha}\right) \\ \Phi\left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_3} - \beta_4 \ln(\tau_3 + t - 400) - \mu_\alpha}{\sigma_\alpha}\right) \\ \Phi\left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_4} - \beta_4 \ln(\tau_4 + t - 531) - \mu_\alpha}{\sigma_\alpha}\right) \\ \Phi\left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_5} - \beta_4 \ln(\tau_5 + t - 750) - \mu_\alpha}{\sigma_\alpha}\right) \end{cases} \quad (20)$$

Equation (20) shows the set of equations for each stress level between 70 °C and 110 °C maintained at specific stress time intervals according to the step-stress ADT design plan illustrated in Fig. 1. The mathematical expression for the probability distribution function (PDF), denoted by $f_{ik}(t)$, was obtained for one stress level at 70 °C for the initial stress duration of 200 hours as shown in (21) by taking the derivative of the CDF expression presented in (19). Similarly, the overall PDF expression for the applied thermal step-stress levels, $f_{ik}(t)$, can be obtained by applying the natural logarithm of the PDF as shown in (22)

$$f_{ik}(t) = \begin{cases} D \exp\left(-\frac{1}{2} \left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3/T - \beta_4 \ln(t) - \mu_\alpha}{\sigma_\alpha}\right)^2\right) \\ \text{where } D = \frac{1}{\sigma_\alpha \sqrt{2\pi}} \end{cases} \quad (21)$$

$$\ln(f_{ik}(t)) = \begin{cases} Z - \frac{1}{2} \left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_1} - \beta_4 \ln(t) - \mu_\alpha}{\sigma_\alpha}\right)^2 \\ Z - \frac{1}{2} \left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_2} - \beta_4 \ln(\tau_2 + t - t_1) - \mu_\alpha}{\sigma_\alpha}\right)^2 \\ Z - \frac{1}{2} \left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_3} - \beta_4 \ln(\tau_3 + t - t_2) - \mu_\alpha}{\sigma_\alpha}\right)^2 \\ Z - \frac{1}{2} \left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_4} - \beta_4 \ln(\tau_4 + t - t_3) - \mu_\alpha}{\sigma_\alpha}\right)^2 \\ Z - \frac{1}{2} \left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T_5} - \beta_4 \ln(\tau_5 + t - t_4) - \mu_\alpha}{\sigma_\alpha}\right)^2 \\ \text{where } Z = -\ln(\sigma_\alpha/\sqrt{2\pi}) \end{cases} \quad (22)$$

The likelihood function (L_f), (23) or in natural logarithm form in (24), for the tested samples at different stress level can be then expressed as the multiplication of the PDF function at specific time intervals, where t_i represents the different EMC performance degradation measurement time at which the EMC degradation data were computed for the tested IC samples (Fig. 8), k refers to the two different voltage stress level, n_k is the number of samples tested at each stress level. The derivative of the analytical expression in (24) with respect to the unknown parameters of the degradation model is essential prior to applying the maximum likelihood estimation (MLE) method. Considering the complexity of the proposed model with multiple unknown parameters, the genetic algorithm was considered for the optimization purposes to predict the unknown parameters. Table III provides the estimated values of the degradation model parameters for both UA78L05 and

TABLE III
DEGRADATION MODEL PARAMETERS FOR BOTH L78L05 AND UA78L05

Degradation model parameters	IC reference	
	UA78L05	L78L05
σ_α	-1.55	-3.43
μ_α	0.54	0.61
β_2	-1.01	-0.22
β_3	116.05	116.04
β_4	0.23	0.20
$L_f(t \sigma_\alpha, \mu_\alpha, \beta_2, \beta_3, \beta_4)$	0.04	0.03

L78L05 tested DUTs. Consequently, the generalized EMC performance degradation model, developed by the ADT modeling approach, would allow to predict the conducted immunity degradation behavior of the the tested IC samples at any known or unknown multiple stress conditions.

$$L_f(t|\mu_\alpha, \sigma_\alpha, \beta_2, \beta_3, \beta_4) = \prod_{k=1}^2 \prod_{i=1}^{n_k} f_{ik}(t_i) \quad (23)$$

$$\ln(L_f(t|\mu_\alpha, \sigma_\alpha, \beta_2, \beta_3, \beta_4)) = \sum_{k=1}^2 \sum_{i=1}^{n_k} \ln(f_{ik}(t_i)) \quad (24)$$

VI. CONCLUSION

This paper develops models for degradation and reliability of pin-to-pin compatible voltage regulators, L78L05 and UA78L05, based on the long-term conducted immunity degradation performance during stress time-dependent ADTs.

The ALT-Weibull reliability modeling approach was considered to develop the reliability model as a function of different G and V stress constraints. The developed ALT model was utilized to predict the unknown model constants of both L78L05 and UA78L05, as well as determine the electromagnetic unreliability (or failure probability) of all the tested samples under the combined effect of different user-defined G and V stress conditions. Unreliability (or failure probability) showed a decreasing trend with increasing G criterion at fixed V overstress level for both L78L05 and UA78L05 tested samples. However, at a higher G criterion level, higher lifetime (i.e., pseudo TTF) was obtained for both UA78L05 and L78L05 samples. Unlike the tested samples of the UA78L05, L78L05 samples exhibited a lower TTF at higher V stress levels when a fixed G criterion was applied to the EMC degradation data. It was found that the pseudo TTF of one of the tested sample of L78L05 for the 10% criterion (around 362 hours at 9 V with 50% unreliability) compared to the tested UA78L05 IC (around 465 hours with 50% failure probability) at the same threshold criterion and voltage stress level. Hence, considering the use of limited sample size, an accurate estimation of the developed ALT-Weibull model could be used to assess the lifetime reliability of regulator ICs with better accuracy, based on the variation in EMC performance under any known or unknown stress conditions.

A physics-based degradation modeling approach was applied to model the monotonic EMC performance degradation at different ADT stress duration to predict the degradation path model parameters as a function of environmental stress conditions specified in the ADT plan. Estimating the unknown

model constants of the developed generalized degradation path model would allow to investigate the gradual conducted immunity degradation behavior of the DUTs under any tested or untested conditions. Although the developed reliability model allow to assess the lifetime reliability of both UA78L05 and L78L05 tested ICs for any defined threshold and voltage stress level, the limitation of such a model is the possibility to independently estimate the acceleration factor due to temperature stress only (Arrhenius model).

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