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High Temperature Accelerated Ageing Influence on the Conducted Immunity Modelling of the Commonly Used Voltage Regulator ICs

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Abstract—This paper aims to develop and compare the integrated circuit conducted immunity (ICIM-CI) models of two different voltage regulator ICs with similar functionality (i.e., UA78L05 and L78L05) under the combined influence of two different electrical overstress (i.e., 9 and 12 V) and high temperature (i.e., 70–110 °C) stresses ageing conditions for a total stress duration of 950 hours. Step-stress accelerated degradation tests (SSADT) are performed on two samples of UA78L05 (i.e., T1 and T2) and L78L08 (i.e., S1 and S2) manufactured by Texas Instrument and STMicroelectronics, respectively. Direct power injection (DPI) test was conducted in nominal conditions (i.e., 7.5 V and 25 °C) on these selected ICs according to IEC 62132-4 standard before and after the accelerated ageing test. For the studied cases, it was found that the passive distribution network (PDN) models extracted before and after ageing test for the ICIM-CI model of UA78L05 and L78L05 remained unaffected. However, the ageing process affected the internal behavioral (IB) block of the ICIM-CI model significantly due to noticeable reduction in the conducted immunity level characterized by the extracted IB look-up table data in terms of power transmitted and frequency. Both fresh and aged samples of L78L05 demonstrated higher conducted immunity profile compared to those of UA78L05.

Index Terms—ICIM-CI; IB; PDN; SSADT; thermal stress; immunity drift

I. INTRODUCTION

Electromagnetic robustness (EMR) of integrated circuit (ICs) is usually affected by ageing under the influence of harsh external environmental stress conditions (i.e., high temperature and electrical overstress) [1]. Accelerated life tests can be performed on integrated circuits (ICs) by applying stress conditions to activate and accelerate the rate of degradation due to intrinsic failure mechanisms induced by ageing [2]. For example, hot carrier injection (HCI) and negative bias transistor instability (NBTI) are known to degrade the electromagnetic compatibility (EMC) performance of ICs [3]. Those

internal degradation mechanisms modify different transistor parameters by lowering the electron mobility and increasing the threshold voltage (V_{th}) of the aged ICs, causing significant impact on electromagnetic emission under the applied electrical stress conditions [4]. Likewise, the influence of ageing can also affect the functionality (e.g. noise, saturation current, signal propagation delay) due to the variation of the physical parameters of the transistors in both digital and analog ICs, resulting significant reduction in the conducted immunity to electromagnetic interferences (EMI) [5], [6].

Accelerated life tests methods, such as, high temperature operating life (HTOL) and low temperature operating life (LTOL), are usually performed on the ICs to evaluate the influence of ageing on the conducted immunity to EMI. According to the AEC-Q100-Rev-F standard, HTOL test is performed by applying constant thermal stress at 150 °C for 450 hours, whereas LTOL test requires applying thermal stress at -40 °C for the same stress period [7]. In [6], HTOL ageing test was performed to characterize the evolution of the ageing induced immunity drift of analog circuit structure (i.e., variable controlled oscillator) designed in 0.25 μm CMOS technology. In [8], accelerated ageing conditions (i.e., electrical overstress) was applied for a specific stress period on the low-dropout voltage regulator (LDO) circuit implemented on a test IC chip to accelerate relevant wear-out degradation mechanisms until the tested chip fails. The changes in the LDO immunity was characterized during the ageing process using the DPI measurements according to the IEC 62132-4 standard [9] prior and after the accelerated life tests, which showed an increase in the electromagnetic immunity drift [8]. Moreover, the long-term conducted immunity of different analog circuit blocks of the phase-locked loop was analyzed by performing the

accelerated life tests, and the results revealed that the ageing reduced the immunity profiles of the tested structures across the whole DPI frequency range [10].

IC designers and manufacturers need to predict the conducted immunity of ICs prior to the manufacturing phase. ICIM-CI model has been proposed and published in the IEC 62433-4 standard [11]. This standard model can be extracted from simulations based on the knowledge about the internal structure of the IC under test. In [12], the effect of ageing and external thermal stress conditions on the proposed ICIM-CI model of a custom-designed integrated oscillator was studied, demonstrating significant reduction of the conducted immunity level with better accuracy that can be taken into account in the future revised version of the ICIM-CI standard. In [13], multi-port conducted immunity model was proposed and compared with the measurements to validate accuracy of the simulation model to estimate the EMC performance of the bandgap reference circuit designed and implemented in the test chip. In [14], the LDO susceptibility model was proposed based on the MOSFET models to extract the ICIM-CI model, which was then validated using the DPI measurements. In [15], the ICIM-CI modeling process was presented by extracting individual models for both linear passive and non-linear active elements of the LDO regulator in order to compare the conducted electric fast transient (EFT) immunity measurement to the proposed simulation model. In [16], a white-box modeling approach was presented for the LDO regulator mounted on a test chip to demonstrate the methodology required to extract the ICIM-CI model. The model was then validated by comparing the simulation results to the DPI measurements. However, the impact of ageing on the ICIM-CI models of ICs should be investigated in order to predict long-term EMR and lifetime reliability. In [17], an electrical simulation model for the voltage regulator as well as an accelerated degradation model were proposed to predict various reliability parameters based on functional performance under different thermal and electrical overstress conditions.

Here, we showcase that the standard ICIM-CI model might be updated and modified to analyze the EMC performance, while taking into account of the influence of accelerated ageing on the conducted immunity model of ICs.

II. MATERIALS AND METHODS

This section presents the test conditions for accelerated aging applied to the chosen voltage regulator ICs. Furthermore, it also introduces the experimental test setup used to conduct high temperature SSADT as well as the DPI test on the ICs to characterize the ageing impact on the developed ICIM-CI models.

A. The Accelerated Ageing Test Plan

The accelerated ageing test plan was designed to investigate and compare the high temperature ageing impact on the EMC performance degradation and the ICIM-CI models of the selected ICs (i.e., UA78L05 and L78L05). Table I provides information on the accelerated ageing test plan, which

TABLE I
DESIGN OF THE ACCELERATED AGEING TEST PLAN

IC reference	Samples	Thermal stress (°C)	Electrical overstress (V)	Total stress duration (hours)
UA78L05	T 1	70-110 °C	9 V	950 hours
	T 2	70-110 °C	12 V	950 hours
L78L05	S 1	70-110 °C	9 V	950 hours
	S 2	70-110 °C	12 V	950 hours

includes the number of IC test samples, total ageing stress duration, electrical overstress and thermal stress conditions applied on the samples. The table demonstrates that identical thermal step-stress conditions were applied to each of the four DUT samples. Two samples (i.e., T1 and S1) of UA78L05 and L78L05, were respectively subjected to a low arbitrary electrical overstress voltage of 9 V (20% higher than nominal voltage). In contrast, high supply voltage stress condition (60% greater than nominal voltage) was chosen for the T2 and S2 samples, ensuring the aged samples remain operational at the end of the ageing test.

B. Measurement Test Setup and Procedures

Four fresh DUT samples were placed inside the climatic chamber (Climat2) to perform high temperature accelerated ageing test for 950 hours. The accelerated ageing test setup is shown in Fig. 1. The test setup consists of high temperature cables (Amphenol-RF 095-902-466-004) to withstand high temperature within the climatic chamber as well as external DC power supply sources for providing electrical overstress above the nominal voltage (i.e., 7.5 V) into the input voltage supply (V_{in}) pin 8 (Fig. 1a) of the tested ICs. Those temperature cables are used to inject the DC input voltage signal to the V_{in} pin of these ICs. The Spirale V software interface integrated with the climatic chamber was used to develop a program for regulating and maintaining the thermal step-stress conditions inside the chamber. The latter consisted of varying the temperature from 70 °C to 110 °C with a linear step increment of 10 °C after every 200 hours, reaching the maximum ageing temperature at 800 hours, and the SSADT was continued for the remaining 150 hours. It should be noted that the maximum temperature stress and total stress duration were chosen based on the operational characteristics of the selected ICs so that the aged samples remain functional avoiding permanent failure throughout the SSADT.

The above-mentioned ageing plan was applied to all the four DUTs in the controlled environment condition for the complete duration of the SSADT induced ageing. The aged samples were removed from the thermal ageing climatic chamber at the end of the process, and the DPI immunity test was performed at the nominal condition (i.e., 7.5 V and 25 °C) in accordance to the IEC 62132-4 standard. The standard DPI test bench was used to perform the DPI experiment, and the relevant



(a)

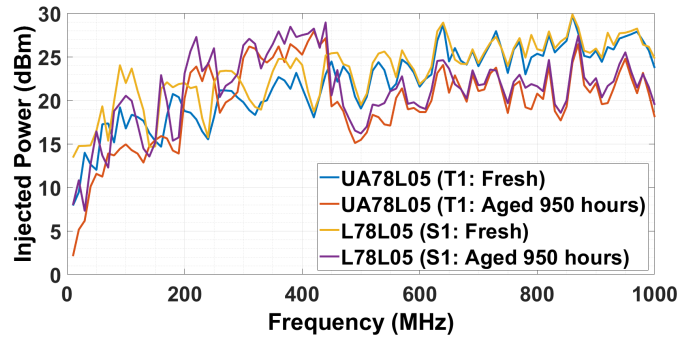


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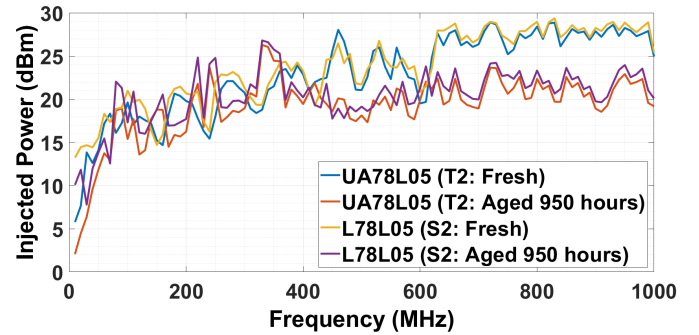
Fig. 1. Accelerated ageing test set-up (a) outside view; (b) inside view of the climatic chamber.

measurement data (i.e., power injected and frequency) were recorded on both fresh and aged IC samples in order to analyze the influence of the aging process on the conducted immunity of the tested ICs.

The DPI measurement setup is similar to that in [18]. The harmonic disturbance signal was injected into the V_{in} pin of each considered sample ICs. Two independent power meters were utilized to record relevant measurement data (i.e., forward power and reflected power). The LabView interface, which is incorporated with the DPI test bench, is programmed to measure the injected power (P_{inj}) when the defined failure threshold criterion is observed at various frequency values. Based on the forward and reflected power measured from the power meters, the minimum P_{inj} required to cause IC malfunction was recorded at each corresponding frequency values over the entire DPI frequency range between 10 and



(a)



(b)

Fig. 2. Ageing impact on the conducted immunity profile of IC samples under same thermal stress and (a) low electrical overstress (i.e., 9 V); (b) high electrical overstress conditions (i.e., 12 V).

1000 MHz. The DPI failure criterion of $\pm 4\%$ deviation from the nominal DC output voltage (V_{out}) was considered on all the test samples. The DC offset voltage (i.e., ± 0.2 V) variation from the nominal V_{out} at the pin 1 (Fig. 1a) of the DUT was considered as the failure threshold. The DPI failure threshold was chosen with a fixed arbitrary value to ensure the ICs remained operational throughout the SSADT, taking into account of various functional performance parameters (i.e., maximum operating temperature, maximum current and operating voltage) of the regulator ICs. It is worth to mention that the input current remained unchanged during the ageing process.

III. RESULTS AND DISCUSSION

This section presents the experimental results to analyze the combined effect of applying thermal and electrical ageing stress conditions on the conducted immunity to EMI. Moreover, several ageing-induced immunity drift parameters (i.e., mean power injection drift, maximum and lowest ageing drift, and standard deviation) for these tested samples were analyzed and compared based on those EMC measurements recorded before and after aging.

A. Accelerated Ageing Impact on Conducted Immunity

The conducted immunity profile for both fresh and aged ICs under two different electrical overstress (i.e., 9 V and 12 V) and identical thermal stress conditions is depicted in Fig. 2.

The ageing impact on the conducted immunity of the samples S1 and T1 subjected to low electrical overstress and high thermal step-stress conditions is displayed in Fig. 2a. Across the whole DPI frequency range, it was found that the fresh L78L05 sample (i.e., S1) was more immune than that of UA78L05 (i.e., T1). Although the conducted immunity profiles for both of these fresh DUT samples showed a gradual increasing trend, the P_{inj} into the V_{in} pin of the S1 sample varied from 12.5 to 25 dBm between 10 and 1000 MHz, while the T1 required lower P_{inj} (i.e., 8 dBm at 10 MHz and 24 dBm at 1000 MHz) to induce the DPI failure. The influence of ageing caused by high temperature and low electrical overstress (i.e., 9 V) conditions resulted in a significant degradation of the conducted immunity level of the tested samples S1 and T1 at both low and high frequency values, ranging from 10 MHz to 200 MHz and 450-1000 MHz, respectively. Conversely, ageing induced by the SSADT and electrical overstress (i.e., 9 V) improved the conducted immunity level of both the aged samples (S1 and T1) in the mid frequency range (i.e., 200–450 MHz). Furthermore, it could be observed that the immunity profile waveform produced for the aged S1 sample needed larger P_{inj} throughout the whole DPI test frequency spectrum than that of the aged T1 sample.

Fig. 2b illustrates the effect of ageing on the conducted immunity level of the test samples (S2 and T2) for the L78L05 and UA78L05, respectively, subjected to both high electrical overstress (i.e., 12 V) and identical thermal stress conditions as outlined in the Table I. Under the effect of the high electrical overstress, both the tested S2 and T2 samples demonstrated a significantly higher difference in the P_{inj} between the aged and fresh states at each corresponding DPI frequencies compared to those of the S1 and T1 samples depicted in the Fig. 2a. Between 10 and 1000 MHz, the sample S2, both in fresh and aged states, could endure greater P_{inj} compared to that of the fresh and aged T2 sample. As a result of this immunity behaviour, it was possible to conclude that the S2 was more immune to the harmonic disturbances than that of the the considered T2 sample.

It is worth mentioning that the observed change of the conducted immunity level could be due to the degradation of the associated CMOS transistors within the tested ICs. Depending on the stress magnitude and duration, the SSADT would activate and accelerate intrinsic degradation mechanisms that could modify the electrical properties (i.e., threshold voltage and charge carrier mobility) of several aged CMOS transistors. Numerous internal CMOS transistors of the aged DUTs could be degraded due to high positive biasing voltage and the biasing current caused by the electrical overstress condition, which would increase the V_{th} and reduce the charge carrier (i.e., holes and electrons) mobility [1]. Thus, a clear relationship between the variations of the physical features of CMOS transistors induced by aging and the conducted immunity level could be established. The influence of ageing on the observed dispersion of the conducted immunity level between the fresh and aged states of the tested samples under the DPI measurements can be a result of the variability of the

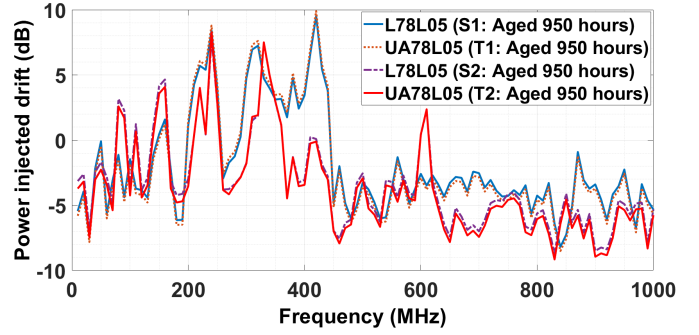


Fig. 3. Influence of the ageing on the conducted immunity drift of the tested ICs.

DUT characteristics and the measurement uncertainty of the DPI test bench equipment.

B. Ageing Induced Conducted Immunity Drift of ICs

The P_{inj} measured for both fresh and aged ICs (i.e., L78L05 and UA78L05) under the nominal conditions were used to evaluate the ageing induced immunity drift threshold, also known as the power injected drift (ΔP_{inj}), by subtracting the measured P_{inj} of the aged from that of the fresh sample. The ageing induced immunity drift of the test samples at each corresponding frequency value is shown in Fig. 3. Negative EMC immunity drift was observed for both aged samples of L78L05 and UA78L05 at the high frequency range (i.e., 650-1000 MHz). Throughout the whole DPI frequency range, both the aged T1 and T2 samples showed slightly higher mean immunity drift than those of the aged S1 and S2. Moreover, positive ΔP_{inj} of the immunity threshold was observed within the specific frequency range (i.e., 250-450 MHz) due to the fact that the measured P_{inj} of the aged sample was higher than that of the fresh IC, highlighting an improvement in the conducted immunity level of all the tested samples. The impact of the high electrical overstress condition on the aged S2 and T2 samples could be noticed in their respective ageing immunity drift waveforms, which are shown in the Fig. 3. The aged S2 sample showed greater ΔP_{inj} immunity drift than the aged S1, indicating higher conducted immunity drift due to the significant influence of the electrical stress observed on the EM immunity of the aged DUT. Likewise, the aged sample T2 demonstrated higher conducted immunity drift level compared to that of the T1 due to observing noticeable difference in the ΔP_{inj} evaluated throughout the whole frequency range.

Table II summarizes ageing induced EMC drift parameters computed for all the distinct samples of ICs (i.e., L78L05 and UA78L05). The absolute mean EMC ageing drift (ΔMP_{inj}) over the entire frequency range is evaluated as the ΔP_{inj} for both the UA78L05 and L78L05 varied at every corresponding frequency value. The ΔMP_{inj} for the aged S1 and S2 samples of was 6.97% and 6.4% lower than those of the aged T1 and T2, respectively. Thus, the L78L05 showed more EM robustness and immunity than the UA78L05 under the indicated accelerated ageing conditions. Due to the effect of the high

TABLE II
AGEING INDUCED IMMUNITY DRIFT PARAMETERS

IC reference	Samples	Absolute mean EMC ageing drift (ΔMP_{inj}) [dB]	Minimum EMC ageing drift ($P_{inj_{MIN}}$) [dB]	Maximum EMC ageing drift ($P_{inj_{MAX}}$) [dB]	Mean standard deviation over all the frequency range (σ) [dB]
UA78L05	T 1	4.31	-8.51	9.90	1.88
	T 2	4.68	-9.15	8.28	2.22
L78L05	S 1	4.01	-8.19	9.54	1.83
	S 2	4.38	-8.72	7.85	2.09

electrical overstress and the defined identical thermal step-stress external factors, the aged S2 and T2 samples exhibited greater immunity drift than the other two aged (S1 and T1) samples. The ΔMP_{inj} of the S2 sample was found to be 9.2% greater than the other DUT of the same IC (i.e., L78L05), with a higher mean standard deviation (σ) of the immunity drift. Similar immunity behaviour was observed for the aged samples of UA78L05, with a 7.9% increase in ΔMP_{inj} for the T2 sample and an 18% higher σ compared to the other aged T1 sample.

IV. EFFECT OF AGEING ON THE ICIM-CI MODEL OF ICs

The ICIM-CI model was developed for both fresh and aged DUT samples in order to compare and analyze the effect of ageing on the conducted immunity of the selected ICs (i.e., UA78L05 and L78L05). To investigate influence of ageing on these ICIM-CI models, both PDN and IB blocks models were extracted from experimental results obtained before and after accelerated ageing tests for each individual DUT of L78L05 and UA78L05. The passive PDN block for each DUT was developed by S-parameter measurements using the vector network analyzer (VNA) similar to that in [19]. The measured reflected coefficient (S_{11}) was used to determine the input impedance (Z_{11}) between the V_{in} and ground (GND) pins of the IC samples before and after accelerated ageing. The PDN block was then modeled by extracting the unknown parameters of the lumped passive components (e.g. resistor, inductor and capacitor) from the Z_{11} profile to investigate the contribution of the ageing effect on the PDN block of the ICIM-CI model. Fig. 4 displays the Z_{11} profile curves versus frequency (i.e., 1–1000 MHz) for both the fresh and aged S1 and T1 test samples. It was found that the impedance profiles of both new and aged ICs remained comparable, with the exception of the aged L78L05 sample (i.e., S1), which exhibited a higher impedance compared to the UA78L05 below and above the resonant frequency, that could be due to higher resistance (R2), lower coupling capacitance (C2), and parasitic inductance (L2) values. As observed in Fig. 4, the extracted RLC values of the PDN model for the aged T1 sample were 35.5 Ω , 19.8 μH and 41.2 pF, whereas the overall RLC values for the aged L78L05 were found to be 49.2 Ω , 21.6 pF and 16.8 μH . The conducted immunity could be similar for both of these tested IC at high frequency due to the small difference in the Z_{11}

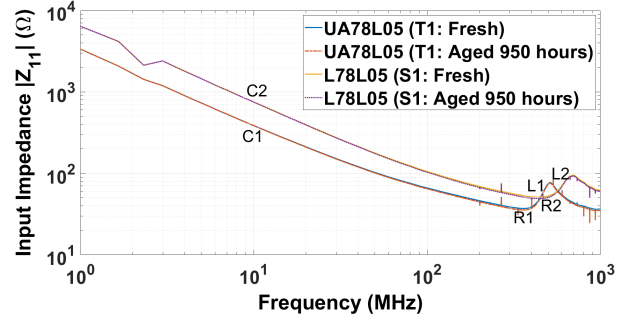


Fig. 4. Influence of the ageing on the input impedance profile of V_{in} of the selected ICs.

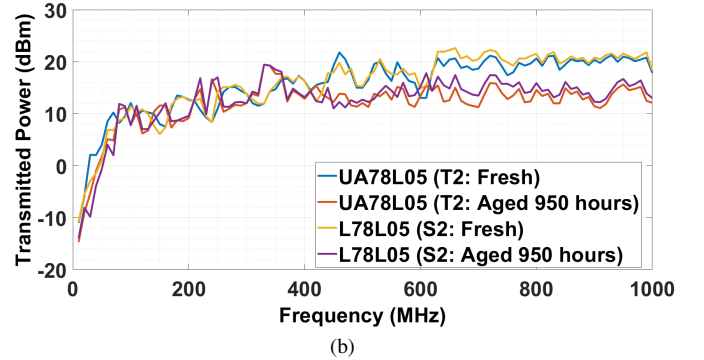
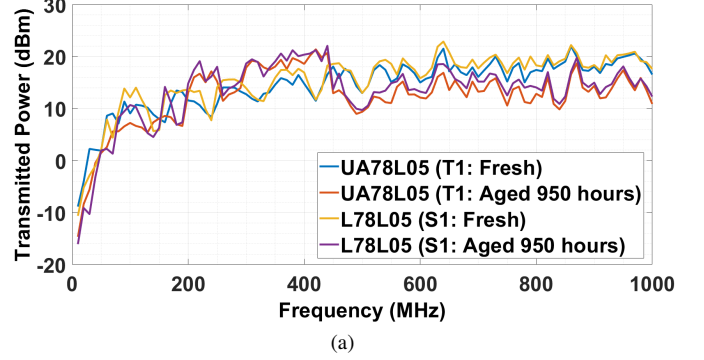


Fig. 5. Influence of ageing on the IB block of the ICIM-CI model of ICs under same thermal stress and (a) low electrical overstress (i.e., 9 V); (b) high electrical overstress conditions (i.e., 12 V).

values dominated by the extracted L1 and L2 values of the PDN block. Note that, the input impedance profiles of the other two IC samples remained constant after being aged at high electrical overstress condition. Thus, it can be concluded that the PDN block of these studied IC samples was unaffected by ageing.

The black box approach was considered to produce the IB block for each individual samples of both UA78L05 and L78L05 by extracting the look-up table from the DPI measurement data. The look-up table data include the actual power transmitted (P_{trans}) to the V_{in} pin under test (PUT) at each corresponding DPI frequency value, causing the DPI failure on the considered IC samples. This P_{trans} corresponds to the actual power that couples into the PUT of the IC mounted on the printed circuit board (PCB), and it is considered as the

relevant parameter for analyzing the conducted immunity level under the influence of ageing. The P_{trans} was evaluated by using the P_{inj} data from the DPI measurements, S_{11} measured using the VNA and insertion loss owing to the cables and PCB trace. The insertion loss was considered to be 3 dB which is subtracted from the P_{inj} to obtain the actual incident power (P_{inc}) at the PUT of the IC. The calculated P_{inc} data was used to evaluate the actual P_{trans} to the IC samples under test ($P_{trans} = [1 - |S_{11}|^2] \times P_{inc}$).

The data from the look-up table, which corresponds to the IB blocks of the ICIM-CI models of L78L05 and UA78L05, was extracted and plotted against the DPI frequency range, as can be seen in Fig. 5. Fig. 5a shows that the P_{trans} of the aged T1 sample decreased by a mean deviation of 4.3 dB and 4 dB for the aged S1 over the whole frequency range. Besides, the maximum P_{trans} deviation between the aged and fresh samples of UA78L05 and L78L05 is 9.9 dB and 9.5 dB, respectively. Similar to the Fig. 5a, Fig. 5b demonstrates that the P_{trans} level of the aged test samples is lower than that of the fresh ones at each corresponding frequency, with the exception between 200 and 400 MHz, which is due to the improvement of the conducted immunity profile due to ageing. Furthermore, the average P_{trans} drift of the aged samples owing to ageing under high electrical stress was 4.4 dB and 4.7 dB for the S2 and T2, respectively. As a result, the reduced P_{trans} level observed in both Figs. 5a and 5b implies that accelerated ageing impacts the extracted IB blocks of the ICIM-CI models of both UA78L05 and L78L05. In order to account for the effect of ageing on the developed ICIM-CI models of the tested IC samples, it is essential to readjust the IB look-up tables with the modified and updated P_{trans} and corresponding frequencies.

V. CONCLUSION

A comparative study was conducted using measurements on the two pin-to-pin compatible voltage regulator ICs (i.e., L78L05 and UA78L05) to examine the effect of thermal and electrical overstress ageing stresses on the developed ICIM-CI models. The DPI experiments were carried out on both fresh and aged ICs. Two different samples of both L78L05 and UA78L05 were aged inside the climatic chamber to accelerate the rate of internal degradation mechanisms (i.e., HCI or/and NBTI) under the combined impact of the defined thermal step-stress and electrical overstress conditions.

The PDN model was developed using the S-parameter measurement and the corresponding input impedance profile of each considered fresh and aged samples. It was found that the PDN model was unaffected by ageing due to observing no variation in the R, L, and C values of the passive elements included in the model.

Before and after the accelerated ageing of the ICs, DPI tests were performed in nominal conditions and measurements were recorded in nominal conditions to extract the look-up table for constructing the IB blocks of individual samples. It was discovered that the ageing reduces the P_{trans} level, resulting in a significant effect on the IB block of both L78L05

and UA78L05 examined samples. Hence, ageing caused by performing the SSADT at the defined stress conditions decreased the conducted immunity of the considered ICs in a given frequency range, with UA78L05 having a higher mean standard deviation of the P_{trans} between fresh and aged samples than the L78L05. To account for the effect of ageing on the IB blocks of the ICIM-CI models of the IC samples under test, the modified P_{trans} values as a function of frequency should be updated in the look-up tables by applying statistical deviations of the ageing immunity drift.

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REFERENCES

- [1] S. Ben Dhia and A. Boyer, “Electro-magnetic robustness of integrated circuits: from statement to prediction,” EMC Compo, Nara, Japan, 2013.
- [2] S. Ben Dhia, A. Boyer, B. Li and A. Cisse Ndoye, “Characteristics of electromagnetic compatibility drifts of nanoscale integrated circuit after accelerated life tests,” IEEE Lett. Electromagn. Compat. Pract. Appl., vol. 46, no. 4, March, 2010.
- [3] B. Li, A. Ndoye, A. Boyer, and S. Ben Dhia, “Characterization of the electromagnetic robustness of a nanoscale CMOS integrated circuit,” EMC Compo 09, Toulouse, France, 2009.
- [4] A. Boyer, S. Ben Dhia, B. Li and N. Berbel, “Experimental investigations into the effects of electrical stress on electromagnetic emission from integrated circuits,” IEEE Trans. Electromagn. Compat., vol. 56, no. 1, Feb. 2014, pp. 44–50.
- [5] R. Fernandez, R. Rodriguez, M. Nafria and X. Aymerich, “Effect of oxide breakdown on RS Latches,” Microelectronics Reliability, vol. 47, Feb. 2007, pp. 581–584.
- [6] B. Li, A. Boyer, S. Ben Dhia and C. Lemoine, “Ageing effect on immunity of a mixed signal IC,” in Proc. Int. Asia-Pac. Symp. Electromagn. Compat., April 12–16, Beijing, China, 2010.
- [7] Automotive Electronics Council, Component Technical Committee, “Stress test qualification for integrated circuits,” AEC-Q100-Rev-F, 2003.
- [8] J. Wu, A. Boyer, J. Li, S. Ben Dhia, and R. Shen, “Characterization of Changes in LDO susceptibility after electrical Stress,” IEEE Trans. Electromagn. Compat., vol. 55, no. 5, Oct. 2013, pp. 883–890.
- [9] Integrated circuits—Measurement of Electromagnetic Immunity 150 kHz to 1 GHz—Part 4: Direct RF Power Injection Method, IEC 62132–4, ed. 1, 2006.
- [10] A. Boyer, S. Ben Dhia, B. Li, C. Lemoine and B. Vignon, “Prediction of a long-term immunity of a phase-locked loop,” Jnl. Electronic Testing, vol. 28, no. 6, pp. 791–802, Nov. 2012.
- [11] IEC 62433-4: integrated circuit—EMC IC modeling—Part 4: Models of Integrated Circuits for EMI behavioral simulation, Conducted Immunity Modeling (ICIM-CI). IEC standard proposal, 2008.
- [12] Q. M. Khan, M. Koohestani, R. Perdriau, J. L. Levant and M. Ramdani, “Validation of IC conducted emission and immunity models including aging and thermal Stress,” IEEE Trans. Electromagn. Compat. (Under Review), 2023.
- [13] S. H. Airieau, T. Dubois, G. Duchamp and A. Durier, “Multi-port ICIM-CI modeling approach applied to a bandgap voltage reference,” in Proc. Int. Symp. Electromagn. Compat. - EMC EUROPE, Nov. 2016, pp. 526–531.
- [14] J. Wu et al., “LDO EMC susceptibility modeling with on-chip sensor measurements,” in Proc. Asia-Pac. Conf. on Environ. Electromagn. (CEEM), Nov. 06–09, Shanghai, China, 2012.
- [15] Y. Huang, J. Wu, C. Li and W. Zhu, “Investigation on EFT effects in a low dropout voltage regulator,” in Proc. Asia Pac. Symp. Electromagn. Compat. (APEMC), 17–21 May, Shenzhen, China, 2016.

- [16] J. Wu et al., "Modeling and simulation of LDO voltage regulator susceptibility to conducted EMI," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 3, Jan. 2014, pp. 726–735.
- [17] J. Al Rashid, L. Saintis, M. Koohestani and M. Barreau, "Coupling simulation and accelerated degradation model for reliability estimation: application to a voltage regulator," *Microelectronics Reliability*, vol. 138, Nov. 2022.
- [18] J. Al Rashid, M. Koohestani, R. Perdriau, L. Saintis and M. Barreau, "Combining obsolescence and temperature stress to evaluate the immunity of voltage regulators to direct power injection in long lifespan systems," *IEEE Lett. Electromagn. Compat. Pract. Appl.*, Early Access, Feb. 2023, DOI: 10.1109/LEMCPA.2023.3240621.
- [19] J. Al Rashid, M. Koohestani, L. Saintis, and M. Barreau, "A State-of-the-Art Review on IC Reliability," *Proc. of the 31st European Safety and Reliability Conf.*, pp. 1850–1857, Angers, France, Sep. 2021.