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Combining Obsolescence and Temperature Stress to Evaluate the Immunity of Voltage Regulators to Direct Power Injection in Long Lifespan Systems

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Abstract—This paper compares the electromagnetic compatibility (EMC) performance of three different voltage regulator ICs (i.e. UA78L05, L78L05 and MC78L05) developed by three different manufacturers, with similar functionality and pin compatibility, under the influence of low and high temperature stress conditions (i.e. $-30\text{ }^{\circ}\text{C}$ and $+100\text{ }^{\circ}\text{C}$). Direct power injection (DPI) was performed on these ICs to analyze the impact of applying thermal stress on the conducted immunity to the injection of single-tone RF disturbance signal. The DPI immunity parameters were measured and recorded in real-time for an incident amplified power, while the ICs were exposed to low and high thermal stress conditions. It was demonstrated that the minimum injected power required to reach the defined failure threshold voltage criterion ($\pm 4\%$) varied over frequency depending on the ICs. Moreover, these functionally identical ICs showed significant evolution of their conducted immunity in all the considered temperatures, depending on their manufacturer. Input impedance curves were monitored at low, high and nominal temperature, showing noticeable decline of impedance at high frequency. Moreover, the equivalent RLC values of the lumped elements (i.e. resistor, inductor and capacitor) were extracted and compared at these aforementioned temperature conditions to model the power supply network impedance for the selected ICs. The immunity behaviour of these ICs was further investigated by generating look up table data from the DPI measurements.

Index Terms—DPI, conducted immunity, obsolescence, thermal stress, failure criterion

I. INTRODUCTION

Integrated circuit (IC) manufacturers face key challenges on assessing and analyzing obsolescence (or second-source) related to the electromagnetic compatibility (EMC) performance of an IC under the influence of the thermal stress conditions. The evolution of the EMC behavior of an IC subjected to external temperature stresses should be taken into consideration to ensure proper functionality and obsolescence management within the lifecycle of that product.

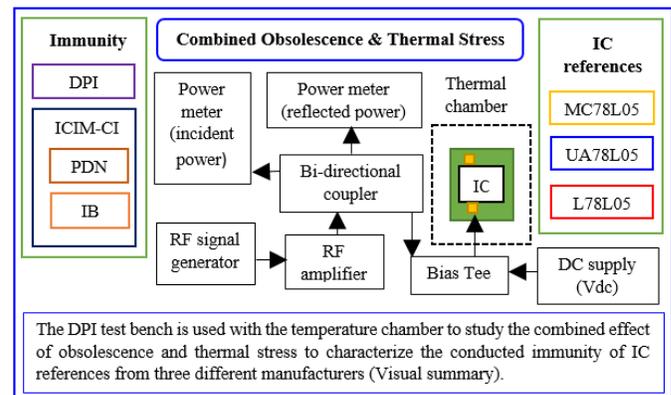
Voltage regulator ICs, which are ubiquitous in almost any electronic application, are likely to be sensitive to electro-

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magnetic interference (EMI) [1]. The conducted immunity of these ICs to EMI can be evaluated by performing testing methods according to the defined EMC standards.

Take-Home Messages:

- A DPI test was conducted on three pin compatible functionally identical voltage regulator ICs under nominal conditions, manufactured by three different companies, demonstrating significant variations in the conducted immunity in different frequency ranges.
- The impact of exposing those ICs to low and high temperatures was found to alter the conducted immunity characterized during the DPI measurement, with the aim to investigate the combined effect of obsolescence (or second-source) management and thermal stress.
- Whatever the IC manufacturers, the DPI characterization results conducted at nominal, extreme low and high thermal stress conditions, revealed a higher immunity of those ICs in extreme temperatures, with marginal difference in magnitude of the minimum injected power (below $+5\text{ dB}$) in high frequency (above 700 MHz).
- The PDN model developed for the considered ICs demonstrated limited information to determine the immunity of the ICs, and the need for an immunity behavior block was shown to be necessary.

Direct Power Injection (DPI) is considered a suitable method to characterize the immunity of ICs with respect to unmodulated radio frequency (RF) sinusoidal signals [2]. According to the IEC 62132-4 standard [3], the DPI test is carried out by injecting single-tone signal disturbances up to

1 GHz into the IC pin in order to record the forward power causing IC failure or malfunction as a function of frequency [4].

Previous research works published on the immunity of low-dropout voltage (LDO) regulator circuits mainly focused on developing a conducted immunity model to predict their EMC performance and validate the developed model by comparing with DPI measurements. In [5], an immunity modeling methodology, compliant with the Integrated Circuit Immunity Model - Conducted Immunity (ICIM-CI) standard [6], was proposed for an entire LDO voltage regulator circuit. In [7], a multiport modeling methodology based on ICIM-CI was proposed and implemented for predicting the conducted immunity of a micro-power voltage bandgap (i.e. LTC1798–2.5) circuit. The proposed model was simulated and the results were compared with the DPI and S -parameter measurements to validate the accuracy of the model. In [8], an on-chip voltage sensor was introduced inside the regulator IC to measure DPI immunity results, and demonstrated the construction of an accurate electrical simulation model based on both off-chip and on-chip measurement data, together with the internal circuit information of the regulator.

External thermal stress factors, such as temperature and humidity, can affect the EMC robustness of ICs throughout their entire lifetime. In [9], the reliability parameters determined from the coupling of the developed simulation and acceleration model for the designed voltage regulator could be compared with the accelerated life test results. Previous research studies intended to address the impact of electrical stress on the evolution of conducted immunity of electronic components [1]. The latter was investigated in [10] for the low-dropout voltage regulator to understand the link between its EMC performance evolution and electrical characteristics. However, the simultaneous evolution of conducted immunity as functions of obsolescence and ageing has not been yet been explored. This paper aims to investigate the impact of applying thermal stress conditions (i.e. temperature) on the EMC performance of three functionally identical regulator ICs from different manufacturers, in order to come to a sensible envelope of the conducted immunity of those ICs at different temperatures, when considering component changes due to obsolescence, or second-sources.

II. MATERIALS AND METHODOLOGY

This section addresses the functionality of the voltage regulator ICs as well as the specific DPI test setup used to perform conducted immunity tests under the thermal stress on three functionally identical and pin-to-pin compatible voltage regulator ICs developed by three different manufacturers.

A. Devices Under Test

Three different types of commercially available voltage regulator IC fabricated by three different manufacturers, with comparable pin configurations, similar packaging and identical functionality (i.e. output voltage of +5 V), were chosen for the purpose of the study to compare conducted immunity level in continuous wave (CW) mode by conducting DPI

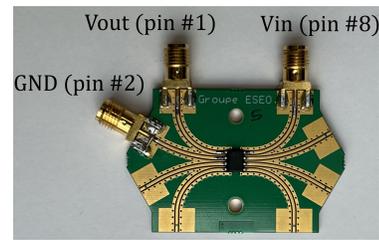


Fig. 1. Voltage regulator IC mounted on a custom DPI test board.

experiment. Those selected ICs with corresponding part or model (i.e. UA78L05, L78L05 and MC78L05) are manufactured by Texas Instruments, ST Microelectronics and On Semiconductor, respectively. Fig. 1 shows one of the tested regulator ICs mounted on a generic SOIC8 extraction test board designed in [11]. The 4-layer FR4 printed circuit board (PCB) design consists of a ground plane for providing ground reference with minimum impedance, short traces with identical length from pads to the board edge connectors to ensure low power loss and low crosstalk during immunity testing of the IC. The following IC pins, i.e. output voltage (pin 1), input voltage (pin 8) and ground (pin 2), were soldered on the PCB traces and SMA connectors were fitted onto the pads corresponding to these pins under test (PUT). Note that, although the internal connections are the same for all those ICs where other grounded pins were internally connected, pins 3, 6 and 7 are not connected to the PCB ground for the ease of experiments, which makes the connection between the die and the PCB ground more resistive and inductive, the main objective being the comparison of the thermal stress impact on the conducted immunity of those ICs. The generic SOIC8 extraction test board design was preferred for the DPI experiment, considering the IC device under test (DUT) has also got the same package, which is also frequently used in ICs for automotive applications.

The functionally identical regulator ICs with exactly similar operational parameters were selected to assess potential obsolescence related EMC issues. Those regulator ICs provide an output voltage of +5 V with an average output current of around 40 mA when a minimum of +7 V input voltage is applied, and can operate within a wide temperature range (i.e. between -40 °C and $+120$ °C). Note that nominal values are the same for all manufacturers.

B. Experimental Setup

The DPI test bench setup is used with the temperature chamber to investigate the combined effect of obsolescence and temperature stress by evaluating the conducted immunity of the selected ICs (as shown in the Visual Summary). It consists of a RF signal generator to generate continuous wave signals with desired power level in the considered frequency range (i.e. 10 MHz–1 GHz with 10 MHz step), a +43 dB gain RF power amplifier with bi-directional coupler, and a wideband external bias tee. The incident power at the output of amplifier was varied from +3 to +33 dBm before injecting into the DUT pin. The bi-directional coupler is connected to a power meter to measure both the incident power of the

amplified RF signals and the reflected power. The bias tee (ZX85-12G-S+), which is used to provide an injection path for the RF signal to couple into the IC pin, includes the coupling capacitor and inductance in a certain configuration such that one end of the inductor is connected to the DC power supply (+12 V) and the other end to the capacitor. Due to its wide bandwidth extending up to 30 GHz, the coupling path between the generator and the PCB has a constant impedance over the injection frequency range. Hence, the output of the bias tee provides the RF disturbance signal coupled to the DC voltage signal, which is injected into the DC input voltage (V_{in}) supply pin of the regulator IC. The corresponding DC output voltage (V_{out}) caused by this disturbance is monitored from pin 1 using a digital oscilloscope. A $\pm 4\%$ criterion on the DC output voltage was considered for positive or negative DPI failure modes. Positive failure mode could be indicated when the positive deviation of +0.2 V (+4%) from the nominal DC output is observed at each DPI frequency values and negative failure mode could be resulted due to the -0.2 V (-4%) variation from the nominal DC output. The algorithm used for conducting the DPI immunity test has been programmed to measure and extract forward power, reflected power and the minimum injected power at each corresponding frequency causing the DPI failure, depending on the immunity or failure threshold defined at the start of the DPI experiment. The numerical data presented in the immunity curves (i.e. Figs. 3 to 5) indicate injected power at the DUTs pin measured against each corresponding frequency, when the DUTs have exceeded the defined failure threshold.

Fig. 2 shows the DPI test bench setup for performing conducted immunity experiments at both considered low and high temperatures. The temperature controlled chamber is used to maintain nominal conditions (+25 °C) or a constant thermal stress (-30 °C and +100 °C) environment. During the DPI experiment, the ICs are placed inside the chamber, and all DPI parameters (i.e. forward power, reflected power, injected power, and frequency) responsible for causing failure are measured and recorded in real-time under all the three aforementioned conditions. Please note that the cables connected with the SMA connectors of the PCB were chosen to withstand extreme high and low temperature [12].

III. RESULTS AND FINDINGS

This section presents the experimental characterization on the conducted immunity due to applying RF signal disturbance on the IC input voltage supply pin in nominal and thermal stress conditions.

A. Conducted Immunity of ICs Under Nominal Conditions

Every IC was tested with an RF signal coupled to the V_{in} pin under nominal conditions. Fig. 3 shows the minimum power injected to the V_{in} pin of the tested ICs (i.e. UA78L05, L78L05 and MC78L05) causing a DPI failure at different frequencies. The immunity profile of the tested ICs demonstrated significant deviation of the injected power throughout the entire frequency range. A comparative study highlighted that the V_{in} pin of L78L05 is the most immune to RF disturbances

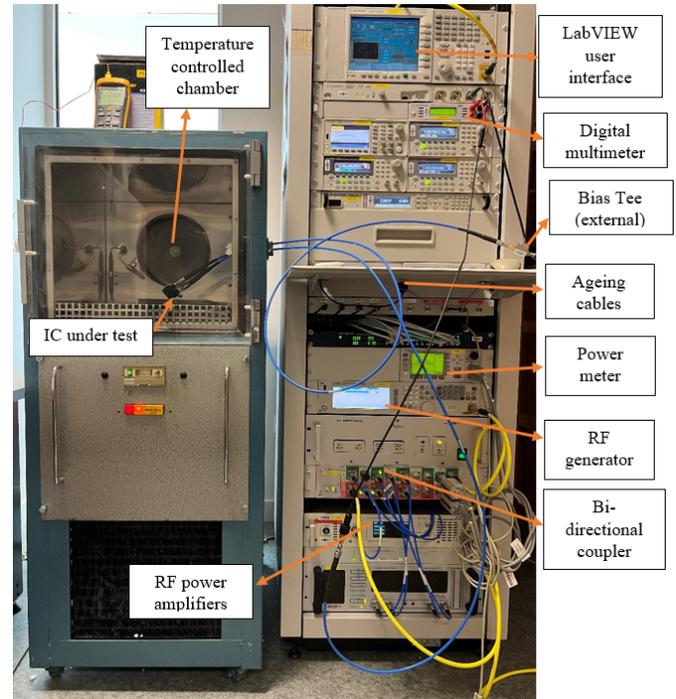


Fig. 2. DPI test bench setup with temperature controlled chamber.

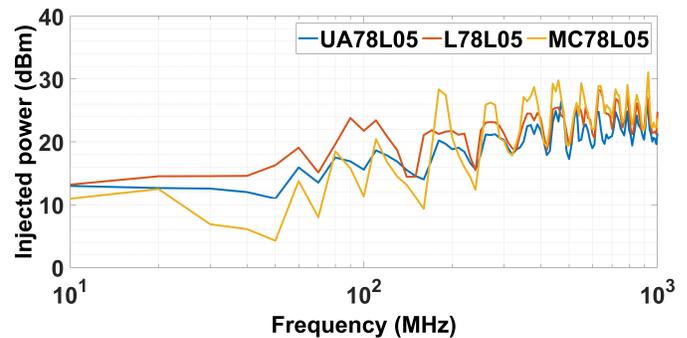


Fig. 3. Incident RF power as a function of frequency at +25 °C.

up to 150 MHz. This study was conducted to compare and assess the immunity profile of these ICs, subjected to both nominal and external thermal stresses. Conversely, the V_{in} pin of MC78L05 was found to be more immune between 300 MHz and 1000 MHz compared to the other two ICs (i.e. UA78L05 and L78L05). Moreover, the DPI immunity profile curve of MC78L05 shows that the measured injected power reached at its peak (i.e. beyond +30 dBm) at 930 MHz, which means this IC could withstand highest injected power causing the DPI failure.

B. Conducted Immunity of ICs Under Thermal Stress Conditions

Experiments were performed on the regulator ICs to investigate the influence of temperature extrema (i.e. -30 °C and +100 °C) on the conducted immunity of the V_{in} pin. The different ICs were first exposed to a temperature stress of -30 °C.

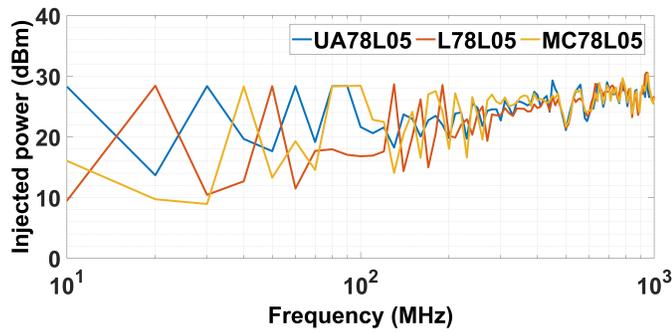


Fig. 4. Incident RF power as a function of frequency at $-30\text{ }^{\circ}\text{C}$.

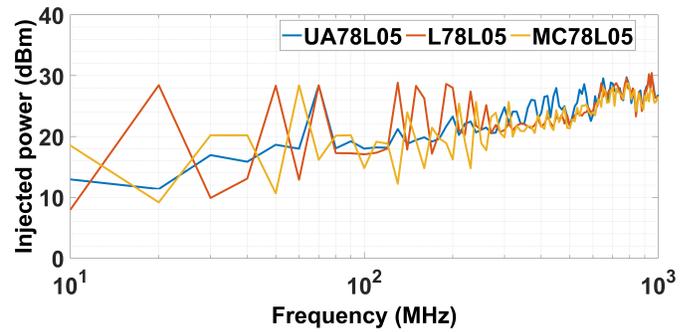


Fig. 5. Incident RF power as a function of frequency at $+100\text{ }^{\circ}\text{C}$.

Fig. 4 compares the impact of the low thermal stress on the three ICs. The MC78L05 was found to be less immune in the low frequency range (from 10–70 MHz). However, this IC was found to be robust and immune to RF disturbances both in the middle and high frequency ranges (from 200–800 MHz). This is because the measured injected power was higher at both high and low immunity points in almost all the corresponding frequency values, except at 550 MHz and 400–450 MHz. Moreover, applying low thermal stress on the UA78L05 resulted to improve the immunity to RF perturbations at low frequency (i.e. $+21.6\text{ dBm}$ against $+18\text{ dBm}$ at 100 MHz).

A similar experimental approach was then followed under the influence of high temperature stress. The recorded injected power to the Vin pin of different ICs at different RF signal frequency is plotted in Fig. 5. Under the influence of high temperature stress, when compared to that of L78L05 and UA78L05 ICs, the Vin pin of the MC78L05 showed a significant decrease in immunity to the RF disturbance throughout the entire frequency range.

The following observations based on the results of the immunity curves displayed in Figs. 4 and 5 can be made:

- 1) within a specific frequency range, each of the selected ICs demonstrated higher DPI immunity both at the low and high temperature stresses when comparing to that of under nominal condition. UA78L05 showed higher immunity both at low and high thermal stress condition throughout the entire frequency range between 10 and 1000 MHz, except at few frequencies (i.e. 20 MHz, 110 MHz and 280 MHz). Between 600 MHz and 1000 MHz, the DPI immunity of L78L05 was found to be greater at both low and high thermal stress scenario. MC78L05 demonstrated higher conducted immunity both at low and high thermal stress conditions than that of nominal condition between 10 MHz and 170 MHz, excluding only few frequency values (i.e. 20 MHz and 110 MHz).
- 2) under the influence of low and high thermal stresses, the Vin pin of all ICs demonstrated higher immunity in the upper frequency range (i.e. 700–1000 MHz).
- 3) all ICs were found to be more immune at low thermal stress than at high thermal stress condition.
- 4) the reason for observing higher DPI immunity both at low and high temperature stress condition could be more likely due to activating and accelerating degradation

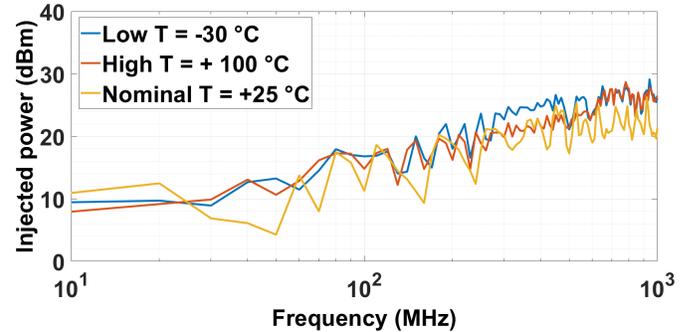


Fig. 6. Minimum immunity of the three regulators under the considered thermal stresses.

mechanisms. At high temperature stress condition, negative bias temperature instability failure mechanism would likely accelerate during the DPI measurements. Hence, the increase in threshold voltage and reduction of charge carrier mobility of transistors might be responsible for the significant variation in the EMC behavior of the ICs. This corroborates the results observed in [13] for different ICs.

Fig. 6 shows the minimum power injected into the Vdd pin which induces a failure in all three temperature conditions regardless of the manufacturers. As can be seen, except below 25 MHz, the immunity seems to be lower in nominal temperature conditions than in both extreme temperatures. Moreover, above 200 MHz, a low temperature stress increases immunity compared to the other conditions. However, even if immunity tends to increase with frequency in all temperature conditions, there are significant differences among the considered ICs (up to $+20\text{ dBm}$ at 20 MHz and below 50 MHz for high and low temperatures, respectively). This highlights the need for characterization of second source ICs in obsolescence studies.

C. *S*-parameters Measurement and Impedance Extraction

In order to verify the obsolescence of the selected ICs and explain possible reasons for significant variations on the EMC performance obtained under nominal conditions, *S*-parameters were measured at nominal temperature to extract the corresponding input impedance observed at the Vin pin. Input Impedance of these ICs were also compared at both lowest and highest temperature (Fig. 7).

Fig. 7a shows the input impedance observed at the Vin pin extracted from the S_{11} parameter. A resonance is observed

above 400 MHz for both MC78L05 and L78L05. However, the UA78L05 showed resonance at around 350 MHz with relatively higher impedance compared to that of MC78L05. The passive distribution network (PDN) model of these ICs consists of resistance (R), package inductance (L) and on-chip capacitance (C) between the V_{in} and ground pins of these ICs [14]. Due to the presence of the wideband bias tee, the interaction with on-chip PDN is expected at frequencies above the DPI range. The equivalent R, L and C values of the PDN model for each individual IC can be extracted analytically from the corresponding input impedance (Z_{11}) profile curve. Table I compares the equivalent RLC values extracted for the PDN models of the selected ICs at low, nominal and high temperature. At the nominal temperature (i.e. $T = +25\text{ }^\circ\text{C}$), the smallest equivalent capacitance for the L78L05 causes lower internal decoupling at low frequencies compared to the other two MC78L05 and UA78L05 ICs. However, the L78L05 shows more immunity to RF disturbances in low frequency (Fig. 3). That means that the immunity behavior (IB) of the active part of the chip should be also considered for a proper evaluation of the IC's immunity. Besides, the package inductance values for the input voltage pin of UA78L05 was found to be higher by 135% and 31.1% compared to that of the MC78L05 and L78L05, respectively, which mainly results in obtaining high input impedance in high frequency. The MC78L05 has the lowest inductance and the highest capacitance at the nominal temperature. Hence, it can be concluded that it is likely to have a larger die, a higher minimum gate length and a smaller bond wire length compared to UA78L05 and L78L05. Likewise, the UA78L05 is not the most immune in high frequency thus requesting a further analysis of the IB.

The transmitted power was further used to assess the IB Table. The IB model information presented in the form of look up table is considered a valid criterion to validate the EMC performance of these ICs. Table II compares the transmitted threshold power P_t among the selected ICs at nominal temperature for different frequencies ranging from 100 to 1000 MHz. The power transmitted to the IB block was evaluated as accurately as possible using the DPI and S_{11} measurements, while taking into consideration the power loss due to the DPI injection path (i.e. bias tee, coupling capacitor, cable and PCB trace). Results provided in Table II shows that P_t is the lowest for the UA78L05 within the considered frequency except at 100 MHz, which validates that the UA78L05 is the least immune to the RF disturbances in that range. However, the L78L05, despite having lower inductance and capacitance values in its PDN, is found to have higher P_t than the UA78L05. This clearly demonstrates that the PDN is not the only block determining the immunity of the whole IC, and that the IB plays an important role. Besides, the MC78L05, with the smallest inductance value, was found to have the highest P_t causing a failure above 200 MHz. Therefore, the IB block determined at the nominal temperature plays significant role to figure out origin of the IC's immunity to the RF disturbances.

In order to investigate the impact of both extreme low and high temperatures on the PDN model of the selected ICs, in terms of their equivalent RLC values, the input impedance

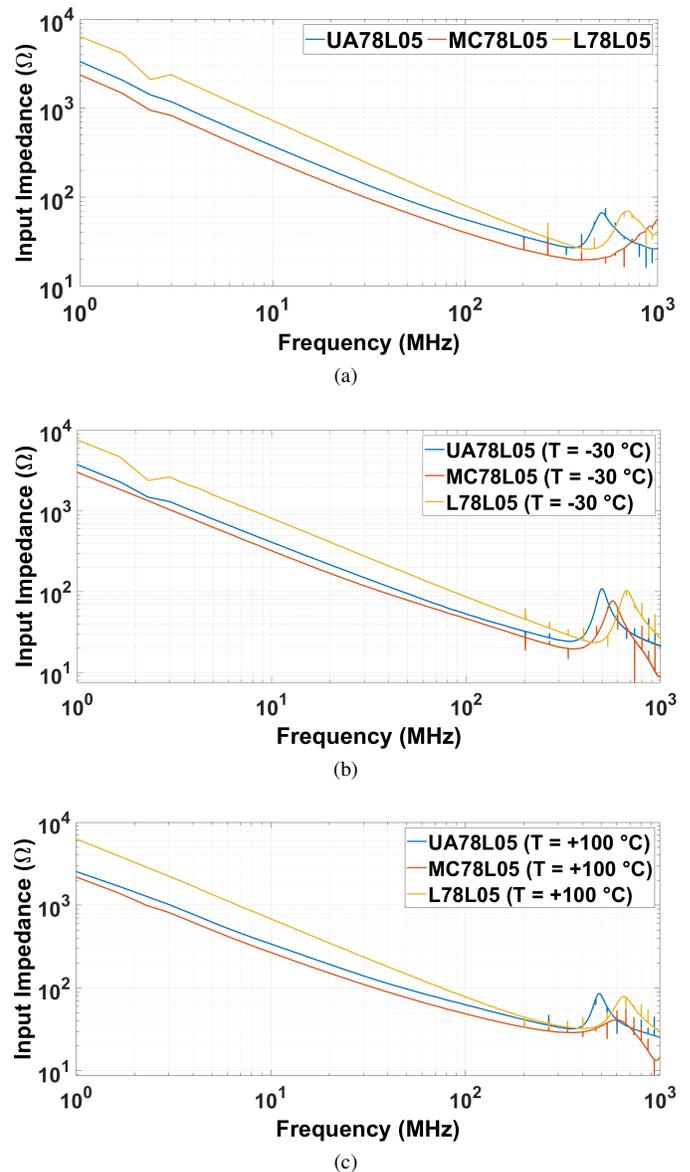


Fig. 7. Input impedance of the tested ICs at different temperatures: (a) $+25\text{ }^\circ\text{C}$; (b) $-30\text{ }^\circ\text{C}$; (c) $+100\text{ }^\circ\text{C}$.

TABLE I
PDN MODEL EXTRACTION FOR THE CONSIDERED ICs AS A FUNCTION OF TEMPERATURE

Temperature (I)	T = -30 °C			T = +25 °C			T = +100 °C		
	R (Ω)	L (μH)	C (pF)	R (Ω)	L (μH)	C (pF)	R (Ω)	L (μH)	C (pF)
UA78L05	24.3	20.3	38.7	27.1	15.6	42.1	32.1	21.01	46.5
MC78L05	19.5	13.8	49.4	19.7	6.63	60.6	28.9	11.1	59.0
L78L05	23.1	13.6	19.6	27.3	11.9	21.8	32.9	15.6	23.3

curves were extracted from the S -parameters measurements as shown in Figs. 7b and 7c, respectively. Fig. 7b depicts that the Z_{11} of the ICs increase in low frequency at the lowest temperature compared to those at the nominal temperature. Besides, the magnitude of the Z_{11} of these ICs is found to be lower in high frequency at the highest temperature. Moreover,

TABLE II
IB LOOK UP TABLE FOR TESTED ICs AT NOMINAL TEMPERATURE

IC reference	UA78L05	MC78L05	L78L05
frequency (MHz)	Transmitted power (dBm)	Transmitted power (dBm)	Transmitted power (dBm)
100	7.45	3.28	10.76
150	6.88	3.44	4.81
200	11.3	13.0	12.78
250	10.51	11.2	13.29
300	13.02	12.75	13.18
350	12.91	19.83	15.24
400	14.91	15.96	16.32
450	18.41	21.29	18.3
500	11.11	13.06	12.78
550	14.24	23.27	18.48
600	12.26	15.64	15.28
650	12.59	20.37	20.99
700	12.66	16.33	15.31
750	13.62	17.14	16.4
800	13.48	19.23	16.53
850	15.93	20.17	17.98
900	12.32	14.76	14.09
950	13.46	16.05	14.41
1000	13.88	17.09	17.26

the Z_{11} curves showed similar decreasing trend throughout the entire frequency range as shown in Figs. 7b and 7c, respectively. The equivalent RLC values extracted at the low and high temperature from the corresponding input impedance curves were found to be comparable and varied considerably as shown in Table I. Based on the Z_{11} curves plotted at -30°C and $+100^\circ\text{C}$, the computed inductance values of UA78L05, MC78L05 and L78L05 increased considerably from its nominal value by 30.1%, 108.1% and 14.3% at -30°C , respectively. Besides, the inductance values evaluated at $+100^\circ\text{C}$ was also incremented for UA78L05, MC78L05 and L78L05 by 34.7%, 67.4% and 31.1%, respectively. The equivalent resistance R values computed from the Z_{11} profile at -30°C were declined from its nominal value by 10.3%, 1% and 15.4% for UA78L05, MC78L05 and L78L05, respectively. On the other hand, the R values extracted at the high temperature were increased by 18.5%, 46.7% and 20.5% in comparison to that of at the nominal temperature for UA78L05, MC78L05 and L78L05, respectively. Under the influence of the lowest temperature, the capacitance value of UA78L05, MC78L05 and L78L05 was reduced from its nominal value by 8.1%, 18.5% and 10.1%, respectively. However, with an exception of MC78L05, whose capacitance value declined by 2.7% at high temperature, UA78L05 and L78L05 demonstrated 10.5% and 6.9% increase of its capacitance from its nominal value, respectively. Hence, these findings suggest that the PDN model plays considerable contribution to characterize the conducted immunity of these ICs at extreme temperatures. Considering the variations of the RLC values from their nominal ones as well as the measured injected power presented in Figs 4 and 5, the IB look up tabular data for MC78L05 show similar decreasing trend at the lowest and highest temperature in high frequencies compared to that of UA78L05 and L78L05; results are not provided for the sake of brevity. The IB model was determined to investigate its role and contribution to the overall immunity of the ICs, along with its PDN model. This assessment could be established under the nominal temperature only, while considering little importance of including the IB table

at extreme temperatures.

IV. CONCLUSION

This paper demonstrated the combined impact of thermal stress and obsolescence by conducting DPI experiments on three functionally identical and pin compatible regulator ICs from three different manufacturers. The selected ICs were exposed to nominal temperature, low and high external temperature conditions (i.e. -30°C and $+100^\circ\text{C}$) during the DPI measurements by injecting the RF disturbance on the input pin of the IC. Based on the defined immunity criterion ($\pm 4\%$), all the ICs under test were measured, yielding either a positive or negative offset voltage at the output pin.

Under the nominal conditions, experimental results demonstrated that, compared to the other two ICs, the MC78L05 had the highest immunity in high frequency. However, that regulator model was found to be less immune to DPI injection when exposed to both low and high thermal stresses. Moreover, regardless of the IC manufacturers, it was observed that the DPI immunity tends to be increased significantly (around +30 dBm at 1000 MHz against almost +10 dBm at 10 MHz) with the increase of frequency at both high and low environmental stress conditions compared to that of the nominal temperatures. These results indicate that it would be essential to verify IC immunity when replacing by a second-source or a more recent device.

Input impedance curves were also compared for all the considered ICs at low, high and nominal temperatures. With the increase of frequency, the impedance curves followed a similar trend but with significant level differences. Package inductance value for UA78L05 was found to be higher than the other two ICs, and the lowest capacitance value was obtained for L78L05. Hence, these RLC variations made it possible to conclude that the UA78L05 was the least immune in high frequency, while the L78L05 showed a high conducted immunity in low frequency. The IB block tabular data of exact transmitted power against frequency was further generated in nominal temperature from the DPI measurements for all the selected ICs. The concluded outcome of observing the highest conducted immunity for MC78L05 compared to the other two ICs was confirmed in high frequency.

Future perspective of this ongoing research work would involve conducting accelerated life tests on these different IC regulators to characterize ageing phenomenon, followed by developing reliability models to integrate with the conducted immunity models to be able to predict the long-term electromagnetic evolution of the immunity parameters as functions of ageing and/or obsolescence.

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REFERENCES

- [1] J. Wu, A. Boyer, J. Li, and S. Ben Dhia, "Characterization of Changes in LDO Susceptibility After Electrical Stress," in *IEEE Trans. Electromag. Compat.*, vol. 55, no. 5, pp. 883-889, 2015, DOI: 10.1109/TEMC.2013.2242471.
- [2] Y. Cheng and S. Hsu, "The direct RF power injection method up to 18 GHz for investigating ICs Susceptibility," *9th Int. Workshop on Electromag. Compat. of Integ. Circuits (EMC Compo)*., Nara, Japan, 2013, DOI: 10.1109/EMCCompo.2013.6735194.
- [3] Integrated Circuits, Measurements of Electromagnetic Immunity 150 kHz to 1 GHz- Part 4: Direct RF Power Injection Method, IEC standard 62132-4, 2006.
- [4] F. Lafon, F. Daran, M. Ramdani, R. Perdriau, and M. Drissi, "Extending the frequency range of the direct power injection Test: uncertainty considerations and modelling approach," *7th Int. Workshop on Electromag. Compat. of Integ. Circuits (EMC COMPO)*., Toulouse, France, 2009, <https://hal.archives-ouvertes.fr/hal-01271861>.
- [5] J. Wu, A. Boyer, J. Li, B. Vrignon, and S. Ben Dhia, "Modeling and simulation of LDO voltage regulator susceptibility to conducted EMI," *IEEE Trans. on Electromag. Compat.*, vol. 56, no. 3, pp. 726-735, 2014, DOI: 10.1109/TEMC.2013.2294951.
- [6] IEC 62433-4: "Integrated Circuit - EMC IC modeling - Part 4: ICIM-CI, Integrated Circuit Immunity Model, conducted Immunity, IEC standard, 2009.
- [7] S. Airieau, T. Dubois, G. Duchamp, and A. Durier, "Multiport ICIM-CI modeling approach applied to a bandgap voltage reference," in *Proc. EMC Europe*., Wroclaw, Poland, 2016, DOI: 10.1109/EMCEurope.2016.7739248.
- [8] W. Jian-fei *et al.*, "LDO EMC Susceptibility Modeling with On-chip Sensor Measurements," *6th Asia-Pacific Conf. on Env. Elec (CEEM)*., Shanghai, China, 2012, DOI: 10.1109/CEEM.2012.6410619.
- [9] J. Rashid, L.Saintis, M. Koohestani and M. Barreau, "Coupling Simulation and Accelerated Degradation Model for Reliability Estimation: Application to a voltage regulator," *Microelectronics Reliability*, Sep 25, 2022, DOI: 10.1016/j.microrel.2022.114682.
- [10] S. Airieau *et al.*, "Effects of ageing on the conducted immunity of a voltage reference: Experimental study and modelling approach," *Microelectronics Reliability*, vol.76-77, pp. 674-679, 2017, DOI: 10.1016/j.microrel.2017.07.030.
- [11] S. T. Op't Land, "Integrated Circuit immunity modelling beyond 1 GHz" PhD dissertation, Univ. of INSA Rennes 1, Rennes, France, 2014.
- [12] Amphenol RF 7029-3531, ATC-PS TEST CBL SMA(M) X2 6FT, Digikey Electronics [Online], Available: <https://www.digikey.fr/fr/products/detail/amphenol-sv-microwave/7029-3531/13919159> , Accessed on: May 10,2022.
- [13] Nestor *et al.*, "Experimental Investigations into the effects of Electrical Stress on Electromagnetic Emission from Integrated Circuits," *IEEE Trans. on Elec. Compat.*, pp. 44-50, 2014, DOI: 10.1109/TEMC.2013.2272195.
- [14] J. Rashid, M. Koohestani, L. Saintis, and M. Barreau, "A State-of-the-Art Review on IC Reliability," *Proc. of the 31st European Safety and Reliability Conf.*., pp. 1850-1857, Angers, France, 2021, <https://hal.univ-angers.fr/hal-03361394>.