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Combining Obsolescence and Temperature Stress to Evaluate the Immunity of Voltage Regulators to Direct Power Injection in a Product Lifecycle

Jaber Al Rashid, Mohsen Koohestani, *Senior Member, IEEE*,
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Abstract—This paper compares the EMC performance of three different voltage regulator ICs (i.e. UA78L05, L78L05 and MC78L05) developed by three different manufacturers, with similar functionality and pin compatibility, under the influence of low and high temperature stress conditions (i.e., $-30\text{ }^{\circ}\text{C}$ and $+100\text{ }^{\circ}\text{C}$). Direct power injection (DPI) was performed on these ICs to analyze the impact of applying thermal stress on the conducted immunity to the injection of harmonic disturbance. The DPI immunity parameters were measured and recorded in real-time for an incident power between -13 and $+30$ dBm, while the ICs were exposed to low and high environmental stress conditions. It was found that the minimum injected power required to reach the defined failure threshold voltage criterion ($+0.20\text{ V}$) varied over frequency depending on the IC reference. Results demonstrated that the L78L05 IC reference was more immune to harmonic disturbance up to around 100 MHz compared to other identical IC references under nominal conditions, but its susceptibility to the EM interference increased above 600 MHz. Moreover, these functionally identical ICs showed significant evolution of their conducted immunity at all considered temperatures, depending on their manufacturer. The outcome of the DPI characterization on these IC references at both low and high thermal stress conditions irrespective of their manufacturers of clearly showed that the DPI immunity improves significantly with increasing frequency compared to that of nominal temperature, with little dispersion on minimum injected power needed to observe failure above 700 MHz. Input impedance curves were plotted at low, high and nominal temperature showed noticeable decline at high frequency, which could also explain the combined impact of temperature and obsolescence on the EMC performance of ICs selected from different manufacturers. Consequently, the equivalent RLC values of the lumped elements (i.e., resistor, inductor and capacitor) were extracted and compared at these aforementioned temperature conditions to model the power supply network impedance for the selected IC references. The immunity behaviour of these ICs were further investigated by generating look up table data from the DPI measurements at nominal temperature.

Index Terms—DPI, conducted immunity, obsolescence, thermal stress, failure criterion

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I. INTRODUCTION

Integrated Circuit (IC) manufacturers face key challenges on assessing and analyzing obsolescence related to the electromagnetic compatibility (EMC) issues under the influence of external environmental stress (i.e., temperature) conditions, which needs to be taken into consideration to ensure proper operation throughout the entire lifecycle of the product. Voltage regulator ICs, which are ubiquitous in almost any electronic application, are likely to be sensitive to electromagnetic interference (EMI) [1]. The conducted immunity of these ICs to EMI can be evaluated by performing testing methods according to the defined EMC standards. Direct Power Injection (DPI) is considered a suitable method to characterize the immunity of ICs in presence of conducted harmonic disturbances propagating in continuous wave (CW) mode [2], [3]. According to the current IEC 62132-4 standard [4], the DPI test is carried out by injecting RF disturbances up to 1 GHz into the IC pin in order to record the forward power causing IC failure or malfunction as a function of frequency.

Take-Home Messages:

- The DPI test conducted on three functionally identical voltage regulator ICs under nominal condition, manufactured by three different companies, demonstrated significant variation in the conducted immunity in different frequency ranges.
- The impact of exposing those ICs to both low and high external temperatures, with the aim to investigate the combined effect of obsolescence (or second-source) and thermal stress, altered the conducted immunity characterized during the DPI measurement.
- Regardless of the IC manufacturers, the DPI characterization result conducted at nominal, extreme low and high thermal stress conditions, revealed that the DPI immunity of ICs follow an increasing trend, and simultaneously the difference in the minimum injected power also reduced (i.e. less than 5 dB) at high frequency (above 700 MHz).
- The PDN model developed for the IC references by extracting the equivalent resistance, inductance and capacitance values demonstrated little information to determine the susceptibility of the whole ICs, and the immunity behavior model also plays a significant role, which has been validated from the observed outcome at the nominal temperature.

Previous research works published on the susceptibility of low-dropout voltage (LDO) regulator circuits mainly focused on developing a conducted immunity model to predict their EMC performance and validate the developed model by comparing with DPI measurements. In [5], an immunity modeling methodology, compliant with the Integrated Circuit Immunity Model - Conducted Immunity (ICIM-CI) standard [6], was proposed for an entire LDO voltage regulator circuit. In [7], a multiport modeling methodology based on ICIM-CI was proposed and implemented for predicting the conducted immunity of a micro-power voltage bandgap reference (LTC1798–2.5) circuit. The proposed model was simulated and the results were compared with the DPI and S -parameter measurements to validate the accuracy of the model. In [8], an on-chip voltage sensor was introduced inside the regulator IC to measure DPI susceptibility results, and demonstrated the construction of an accurate electrical simulation model based on both off-chip and on-chip measurement data, together with the internal circuit information of the regulator.

External environmental stress factors, such as temperature and humidity, can affect the EMC robustness of ICs throughout their entire lifetime. In [9], the reliability parameters determined from the coupling of the developed simulation and acceleration model for the designed voltage regulator could be compared with the accelerated life test results. Previous research studies intended to address the impact of electrical stress on the evolution of conducted immunity [1], [10]. However, the simultaneous evolution of conducted immunity as functions of obsolescence and ageing has not been yet been explored. This paper aims to investigate the impact of applying environmental stress conditions (i.e., temperature) on the EMC performance of three functionally identical regulator ICs from different manufacturers, in order to come to a sensible envelope of the conducted immunity of those ICs at different temperatures, when considering component changes due to obsolescence, or second-sources.

II. MATERIALS AND METHODOLOGY

This section addresses the functionality of the voltage regulator ICs as well as the specific DPI test setup used to perform conducted immunity tests under the thermal stress on three functionally identical and pin-to-pin compatible voltage regulator ICs developed by three different manufacturers.

A. Devices Under Test

Three different types of commercially available voltage regulator IC fabricated by three different manufacturers, with comparable pin configurations, similar packaging and identical functionality (i.e., output voltage of +5 V), were chosen for the purpose of the study to compare conducted susceptibility level in continuous wave (CW) mode by conducting DPI experiment. Those selected IC references (UA78L05, L78L05 and MC78L05) are manufactured by Texas Instruments, ST Microelectronics and On Semiconductor, respectively. Fig. 1 shows one of the tested regulator ICs mounted on a generic SOIC8 extraction test board designed in [11]. The 4-layer FR4 printed circuit board (PCB) design consists of a ground plane

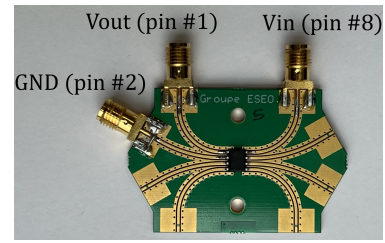


Fig. 1. IC under test.

for providing ground reference with minimum impedance, short traces with identical length from pads to the board edge connectors to ensure low power loss and low crosstalk during immunity testing of the IC. The following IC pins, i.e., output voltage (pin 1), input voltage (pin 8) and ground (pin 2), were soldered on the PCB traces and SMA connectors were fitted onto the pads corresponding to these pins under test (PUT). The generic SOIC8 extraction test board design was preferred for the DPI experiment, considering the IC device under test (DUT) has also got the same package, which is also frequently used in ICs for automotive applications.

The functionally identical regulator ICs with exactly similar operational parameters were selected to assess potential obsolescence related EMC issues. Those regulator ICs provide an output voltage of +5 V with an average output current of around 40 mA when a minimum of +7 V input voltage is applied, and can operate within a wide temperature range (i.e., between -40 °C and $+120$ °C). Note that nominal values are the same for all manufacturers.

B. Experimental Setup

Fig. 1 exhibits the block diagram for the DPI test bench setup. It consists of a RF signal generator to generate continuous wave signals with desired power level in the considered frequency range (i.e., 10 MHz–1 GHz), a +43 dB gain RF power amplifier with bi-directional coupler, and a wideband external bias tee. The bi-directional coupler is connected to a power meter to measure both the incident power of the amplified RF signals and the reflected power. The bias tee includes the coupling capacitor and inductance in a certain configuration such that one end of the inductor is connected to the DC power supply (12 V) and the other end to the capacitor. Hence, the output of the bias tee provides the RF disturbance signal coupled to the DC voltage signal, which is injected into the DC input voltage (V_{in}) supply pin of the regulator IC. The corresponding DC output voltage (V_{out}) caused by this disturbance is monitored from pin 1 using a digital oscilloscope. A $\pm 4\%$ criterion on the DC output voltage was considered for positive or negative DPI failure modes.

Fig. 3 shows the DPI test bench setup for performing conducted immunity experiments at both considered low and high temperatures. The temperature controlled chamber is used to maintain nominal conditions ($+25$ °C) or a constant thermal stress (-30 °C and $+100$ °C) environment. During the DPI experiment, the ICs are placed inside the chamber, and all DPI parameters (i.e., forward power, reflected power, injected power, and frequency) responsible for causing failure

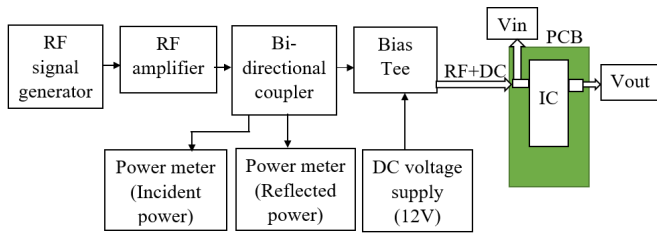


Fig. 2. DPI measurement diagram of an IC.

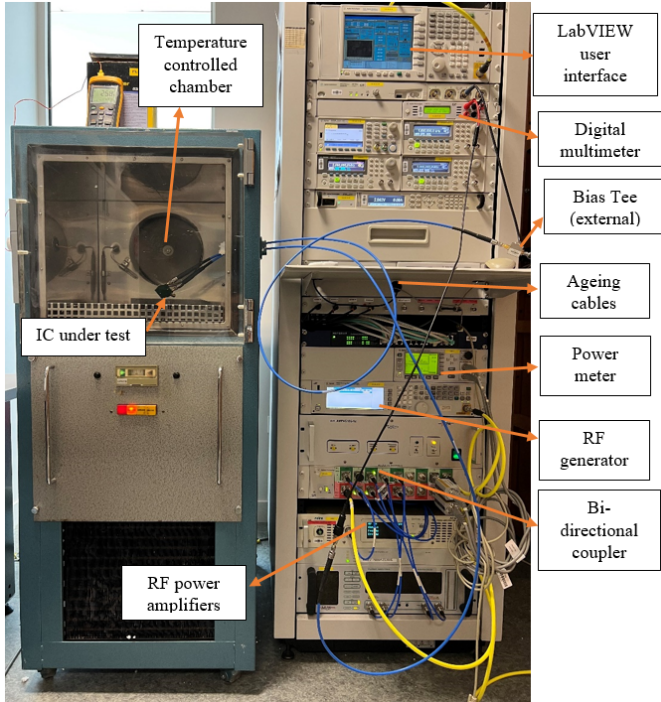


Fig. 3. DPI test bench setup with temperature controlled chamber.

are measured and recorded in real-time under all the three aforementioned conditions. Please note that the cables connected with the SMA connectors of the PCB were chosen to withstand extreme high and low temperature [12].

III. RESULTS AND FINDINGS

This section presents the experimental characterization on the conducted susceptibility due to applying harmonic disturbance on the IC input voltage supply pin in nominal and thermal stress conditions.

A. Conducted Immunity of ICs Under Nominal Conditions

Each of the three different IC regulator references were tested with EM harmonic disturbance coupled to the Vin pin under nominal conditions. Fig. 4 shows the minimum injected power to the Vin pin of the tested ICs references (UA78L05, L78L05 and MC78L05) causing a DPI failure at different frequencies. The immunity profile of the tested ICs demonstrated that the injected power varied abruptly throughout the entire frequency range (10–1000 MHz). A comparative study highlighted that the Vin pin of L78L05

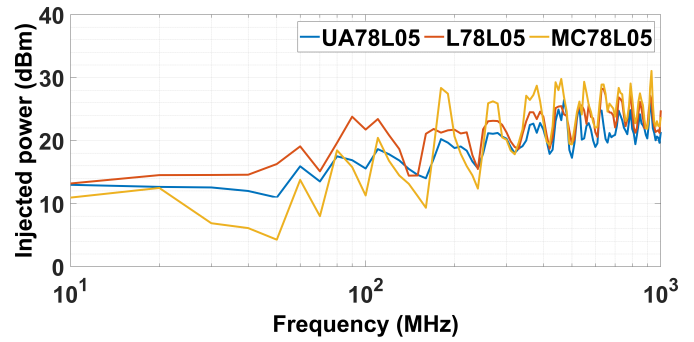


Fig. 4. Immunity profile of different IC references under nominal temperature conditions.

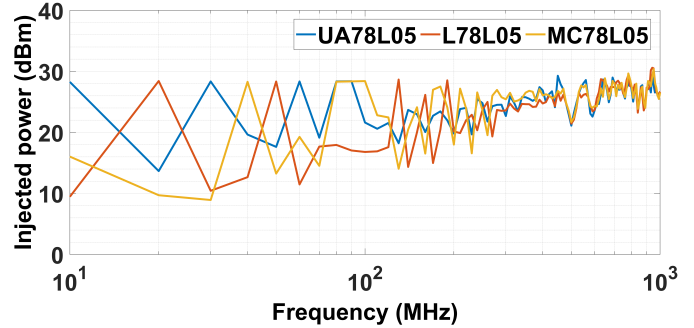


Fig. 5. DPI immunity curves of different IC references under low temperature stress.

found to be the most immune to harmonic disturbances up to 70 MHz. Conversely, the Vin pin of MC78L05 was found to be less susceptible above 300 MHz (+28 dBm) compared to the other two references.

B. Conducted Immunity of ICs Under Thermal Stress Conditions

Experiments were performed on the regulator ICs to investigate the influence of temperature extrema (i.e., $-30\text{ }^{\circ}\text{C}$ and $+100\text{ }^{\circ}\text{C}$) on the conducted immunity of the Vin pin. The different IC references were first exposed to a temperature stress of $-30\text{ }^{\circ}\text{C}$.

Fig. 5 compares the impact of the low thermal stress on the three IC references. The MC78L05 was found to be more susceptible in the low frequency range (from 10–70 MHz). However, this IC was found to be robust and immune to harmonic disturbances both in the middle and high frequency ranges (200–800 MHz). Moreover, applying low thermal stress on the UA78L05 resulted to improve the immunity to RF perturbations at low frequency (i.e., 21.62 dBm against 18 dBm at 100 MHz).

A similar experimental approach was then followed under the influence of high temperature stress. The recorded injected power to the Vin pin of different ICs at different RF signal frequency is plotted in Fig. 6. Under the influence of high temperature stress, when compared to that of L78L05 and UA78L05 IC references, the Vin pin of the MC78L05 showed a significant decrease in immunity to the RF disturbance throughout the entire frequency range.

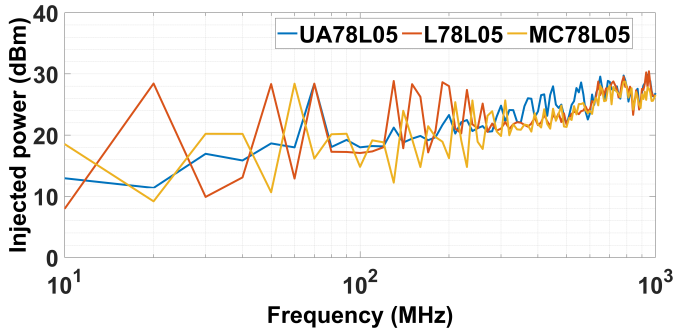


Fig. 6. DPI immunity curves for ICs references at high temperature stress.

The following observations based on the results of the immunity curves displayed in Figs. 5 and 6 can be made:

- 1) whatever the frequency, each of the selected IC references demonstrated higher DPI immunity both at the low and high temperature stresses when comparing to that of under nominal condition.
- 2) under the influence of low and high thermal stresses, the Vin pin of all ICs demonstrated higher immunity in the upper frequency range (i.e., 700–1000 MHz).
- 3) all ICs were found to be less susceptible at low thermal stress than at high environmental temperature stress condition.
- 4) the reason for observing higher DPI immunity both at low and high temperature stress condition could be more likely due to activating and accelerating degradation mechanisms. At high temperature stress condition, negative bias temperature instability failure mechanism would likely accelerate during the DPI measurements. Hence, the increase in threshold voltage and reduction of charge carrier mobility of transistors might be responsible for the significant variation in the EMC behavior of the ICs. This corroborates the results observed in [13] for different ICs.

Fig. 7 shows the minimum power injected into the Vdd pin which induces a failure in all three temperature conditions regardless of the manufacturers. As can be seen, except below 20 MHz, the immunity seems to be lower in nominal temperature conditions than in both extreme temperatures. Moreover, above 200 MHz, a low temperature stress decreases susceptibility compared to the other conditions. However, even if immunity tends to increase with frequency in all temperature conditions, there are significant differences among the considered IC references (up to +20 dBm at 20 MHz and below 50 MHz for high and low temperatures, respectively). This highlights the need for characterization of second source ICs in obsolescence studies.

C. S-parameter Measurement and Impedance Extraction

In order to verify the obsolescence of the selected ICs and explain possible reasons for significant variations on the EMC performance obtained under nominal conditions, S-parameters were measured at nominal temperature to extract the corresponding input impedance observed at the Vin pin.

Fig. 8 shows the input impedance observed at the Vin pin extracted from the S_{11} parameter. A resonance is observed

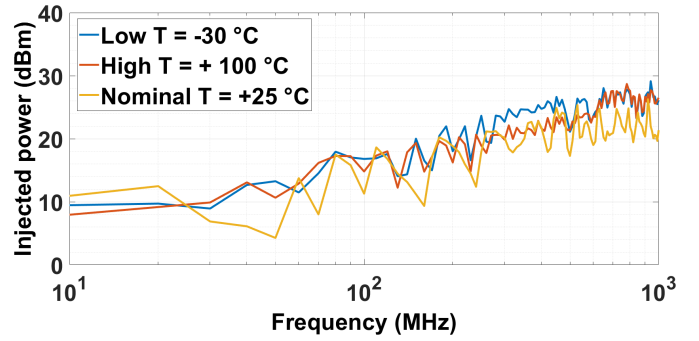


Fig. 7. Minimum injected power for different thermal stresses regardless of the IC manufacturers.

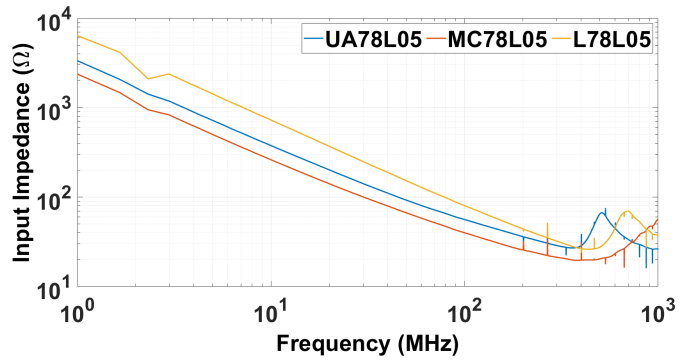


Fig. 8. Input impedance at nominal temperature.

above 400 MHz for both MC78L05 and L78L05. However, the UA78L05 showed resonance at around 350 MHz with relatively higher impedance compared to that of MC78L05. The passive distribution network (PDN) model of these IC references consists of resistance (R), package inductance (L) and on-chip capacitance (C) between the Vin and ground pins of these ICs [14]. The equivalent R, L and C values of the PDN model for each individual IC reference can be extracted analytically from the corresponding input impedance (Z_{11}) profile curve. Table I compares the equivalent RLC values extracted for the PDN models of the selected IC references at low, nominal and high temperature. At the nominal temperature (i.e., $T = +25\text{ }^{\circ}\text{C}$), the smallest equivalent capacitance for the L78L05 causes lower internal decoupling at low frequencies compared to the other two MC78L05 and UA78L05 IC references. However, the L78L05 shows more immunity to harmonic disturbances in low frequency (Fig. 4). That means that the immunity behavior (IB) of the active part of the chip should be also considered for a proper evaluation of the IC's immunity. Besides, the package inductance values for the input voltage pin of UA78L05 was found to be higher by 135% and 31.1% compared to MC78L05 and L78L05, respectively, which mainly results in obtaining high input impedance in high frequency. The MC78L05 has the lowest inductance and the highest capacitance at the nominal temperature. Hence, it can be concluded that it is likely to have a larger die, a higher minimum gate length and a smaller bond wire length compared to UA78L05 and L78L05. Likewise, the UA78L05 is not the most immune in high frequency thus requesting a

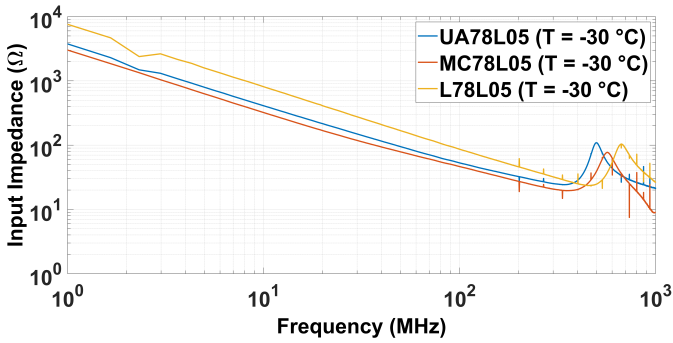


Fig. 9. Input impedance at low temperature.

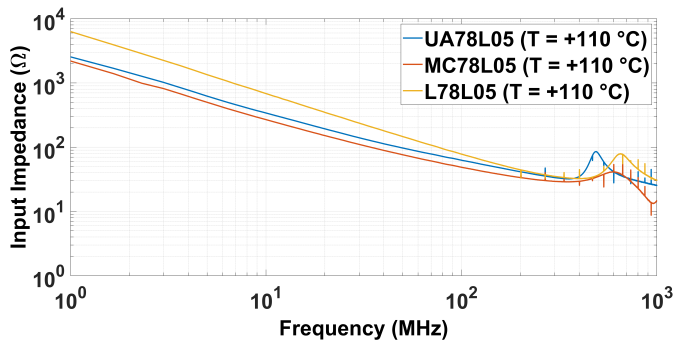


Fig. 10. Input impedance at high temperature.

further study of the IB.

For the sake of completeness, the transmitted power was used to assess the IB Table. The IB model information presented in the form of look up table is considered a valid criterion to validate the EMC performance of these IC references. Table II compares the transmitted threshold power P_t among the selected IC references at nominal temperature for different frequencies between 100 MHz and 1000 MHz and the considered criterion. The power transmitted to the IB block was evaluated as accurately as possible using the DPI measurements, power loss due to the DPI injection path (i.e., bias tee, coupling capacitor, cable and PCB trace) and S_{11} . Results provided in Table II show that P_t is the lowest for the UA78L05 within the considered frequency except at 100 MHz, which validates that the UA78L05 is the most susceptible to harmonic disturbances in that range. However, the L78L05, despite having lower inductance and capacitance values in its PDN, is found to have higher P_t than the UA78L05. This clearly demonstrates that the PDN is not the only block determining the susceptibility of the whole IC, and that the IB plays an important role. Besides, the MC78L05, with the smallest inductance value, was found to have the highest P_t causing a failure above 200 MHz.

In order to investigate the impact of both extreme low and high temperature on the PDN model of the IC references, in terms of their equivalent RLC values, the input impedance curves were extracted from the S-parameter measurements as shown in Figs. 9 and 10 respectively. Fig. 9 shows that the Z_{11} of the IC references increased at the low frequency compared to that of at the nominal temperature and vice versa. However,

TABLE I
PDN MODEL EXTRACTION FOR IC REFERENCES VERSUS TEMPERATURE

Temperature (T)	T = -30 °C			T = +25 °C			T = +100 °C		
	R (Ω)	L (μH)	C (pF)	R (Ω)	L (μH)	C (pF)	R (Ω)	L (μH)	C (pF)
UA78L05	24.3	20.3	38.7	27.1	15.6	42.1	32.1	21.01	46.5
MC78L05	19.5	13.8	49.4	19.7	6.63	60.6	28.9	11.1	59.0
L78L05	23.1	13.6	19.6	27.3	11.9	21.8	32.9	15.6	23.3

TABLE II
IB LOOK UP TABLE FOR IC REFERENCES AT NOMINAL TEMPERATURE

IC reference	UA78L05	MC78L05	L78L05
frequency (MHz)	Transmitted power (dBm)	Transmitted power (dBm)	Transmitted power (dBm)
100	7.45	3.28	10.76
200	11.3	13	12.78
300	13.02	12.75	13.18
400	14.91	15.96	16.32
500	11.11	13.06	12.78
600	12.26	15.64	15.28
700	12.66	16.33	15.31
800	13.48	19.23	16.53
900	12.32	14.76	14.09
1000	13.88	17.09	17.26

the magnitude of the Z_{11} at both low and high temperature was found to be lower than that of at the nominal temperature. Moreover, the Z_{11} curves showed similar decreasing trend throughout the entire frequency range as shown in Figs. 9 and 10 respectively. The equivalent RLC values extracted at the low and high temperature from the corresponding input impedance curves were found to be comparable and varied considerably as shown in the Table I. Based on the Z_{11} curves plotted at -30 °C and $+110$ °C, the computed inductance values of UA78L05, MC78L05 and L78L05 increased considerably from its nominal value by 30.1%, 108.1% and 14.3% at -30 °C. Besides, the inductance values evaluated at $+110$ °C also incremented for UA78L05, MC78L05 and L78L05 by 34.6%, 67.4% and 31.1% respectively. The equivalent R value computed from the Z_{11} profile at -30 °C declined from its nominal value by 10.3%, 1.01% and 15.4% for UA78L05, MC78L05 and L78L05 respectively. On the other hand, the resistance value of the PDN model extracted at the high temperature increased by 18.5%, 46.7% and 20.5% in comparison to that of at the nominal temperature for UA78L05, MC78L05 and L78L05 respectively. Under the influence of low and high temperature, the capacitance value of UA78L05, MC78L05 and L78L05 reduced from its nominal value by 8.08%, 18.5% and 10.1% respectively. However, With an exception of MC78L05, whose capacitance value declined by 2.7% at high temperature, UA78L05 and L78L05 demonstrated 10.5% and 6.9% increase of its capacitance respectively from its nominal value. Hence, these findings suggest that even though the RLC values varies at both low and high temperature, the PDN model has little contribution to the susceptibility of the considered IC references as the conducted immunity characterized in terms of the injected power remains unchanged, Therefore, the IB block determined at the nominal temperature plays significant

role to figure out the origin of the susceptibility IC.

IV. CONCLUSION

This paper investigated the combined impact of thermal stress and obsolescence by conducting DPI experiments on three functionally identical and pin compatible regulator IC references from three different manufacturers. The selected ICs were exposed to nominal temperature, low and high external temperature conditions (i.e., $-30\text{ }^{\circ}\text{C}$ and $+100\text{ }^{\circ}\text{C}$) during the DPI measurements by injecting the harmonic disturbance on the input voltage pin of the IC. Based on the defined fixed failure threshold or immunity criterion (0.20 V), all the ICs under test were monitored to observe monitor either positive or negative failure offset voltage at the output pin. Under the nominal condition, experimental results revealed that the MC78L05 showed least susceptibility to the injection of RF signal at high frequency. However, this regulator model was found to be less immune to DPI injection when exposed to both low and high thermal stress. Moreover, regardless of the IC manufacturers, it was observed that the DPI immunity tends to be increase significantly (around 30 dBm at 1000 MHz against almost 10 dBm at 10 MHz) with increasing frequency at both high and low environmental stress conditions compared to that of in nominal temperatures stress. These results could give us the perspective that it would be essential to replace less immune and an obsolete IC by another with higher DPI immunity and robustness.

Input impedance (Z_{11}) curves were compared for all the considered IC references at low, high and nominal temperature. With increasing frequency, these impedance curves followed similar decreasing trend and significant differences were observed. Lumped elements (i.e., RLC) were considered to model the power supply network impedance between the Vin pin and GND pin of the selected ICs. Package inductance value for UA78L05 was found to be higher than the other two ICs, and the least capacitance value was obtained for L78L05. Hence, these RLC variations allowed us to conclude that the UA78L05 was least immune in high frequency, while the L78L05 showed high conducted immunity in low frequency. The IB block tabular data of exact transmitted power against frequency was generated from the DPI measurements for all the selected IC references. Tabular data results confirmed the expected outcome of observing highest conducted immunity to RF disturbances by MC78L05 compared to the other two IC references in both mid and high frequency. Further analysis on electromagnetic compatibility, such as modeling the IC, might be required to explain these observations through simulations to verify impact of thermal stress and obsolescence of ICs when dealing EMC related issues.

Future perspective of this ongoing research work would involve conducting accelerated life tests to ensure ageing on these different IC regulators, followed by extraction of the DPI immunity parameters under the influence of thermal stress conditions. Later on, conducted DPI models would be developed and simulated to validate the evolution of the immunity parameters as a functions of ageing and/or obsolescence.

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